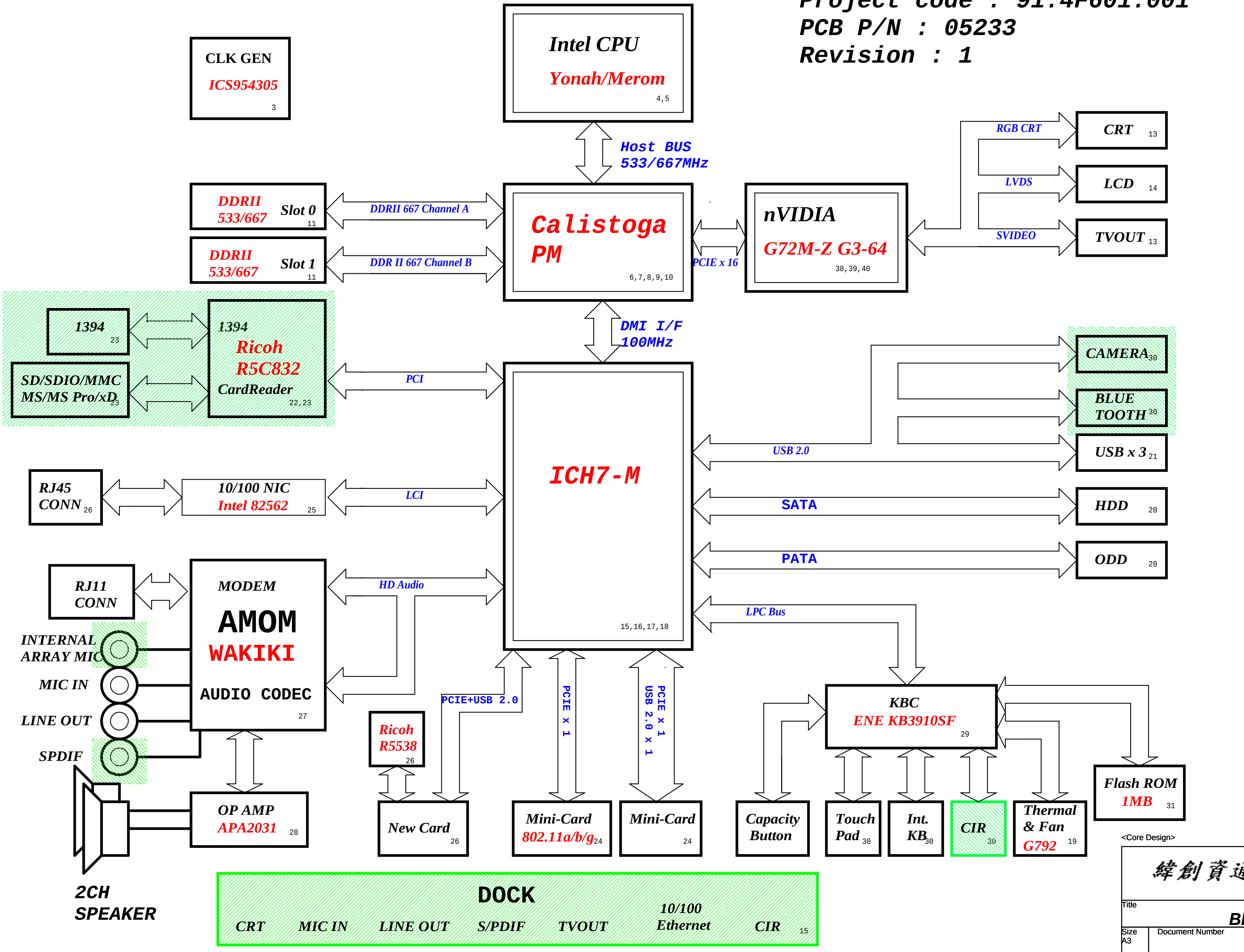
KAI Block Diagram

Project code : 91.4F601.001
PCB P/N : 05233
Revision : 1



SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC
MAX8743

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC
MAX8736ETL

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4
L7: GND
L8: Signal 5

<Core Design>

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Title: **Block Diagram**
Size: A3 | Document Number: KAI | Rev: 1
Date: Wednesday, April 19, 2006 | Sheet 1 of 44

Calistoga Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ICS954305 Spread Spectrum Select

page 3

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.5
0	0	0	1	-1.0
0	0	1	0	-1.5
0	0	1	1	-2.0
0	1	0	0	-0.75
0	1	0	1	-1.25
0	1	1	0	-1.75
0	1	1	1	-2.25
1	0	0	0	+/-0.25
1	0	0	1	+/-0.5
1	0	1	0	+/-0.75
1	0	1	1	+/-1.0
1	1	0	0	+/-0.25
1	1	0	1	+/-0.5
1	1	1	0	+/-0.75
1	1	1	1	+/-1.0

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

ICH7M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

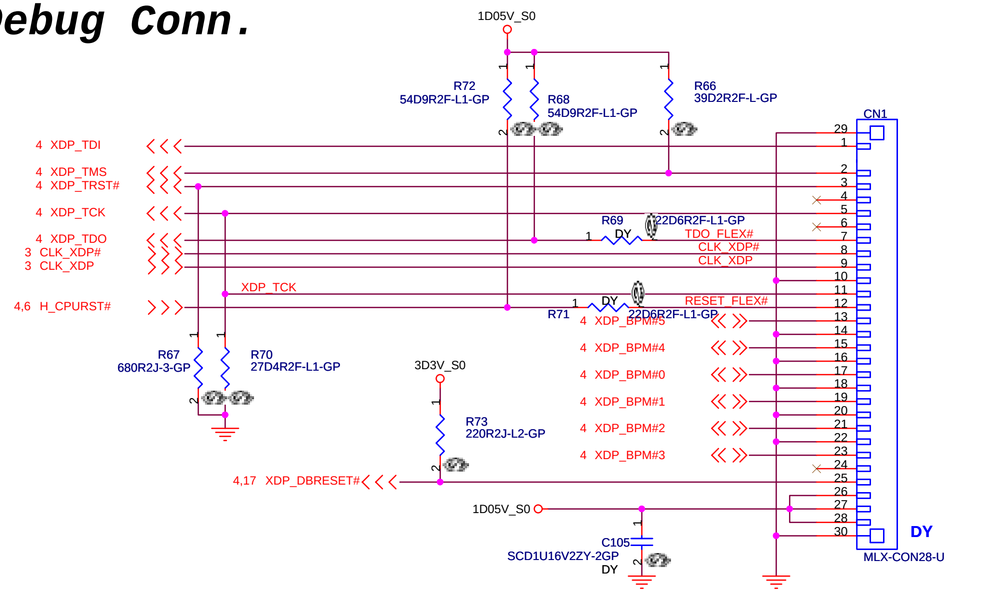
ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

History

11.18.2004: mini card not ready

ITP Debug Conn.



<Core Design>

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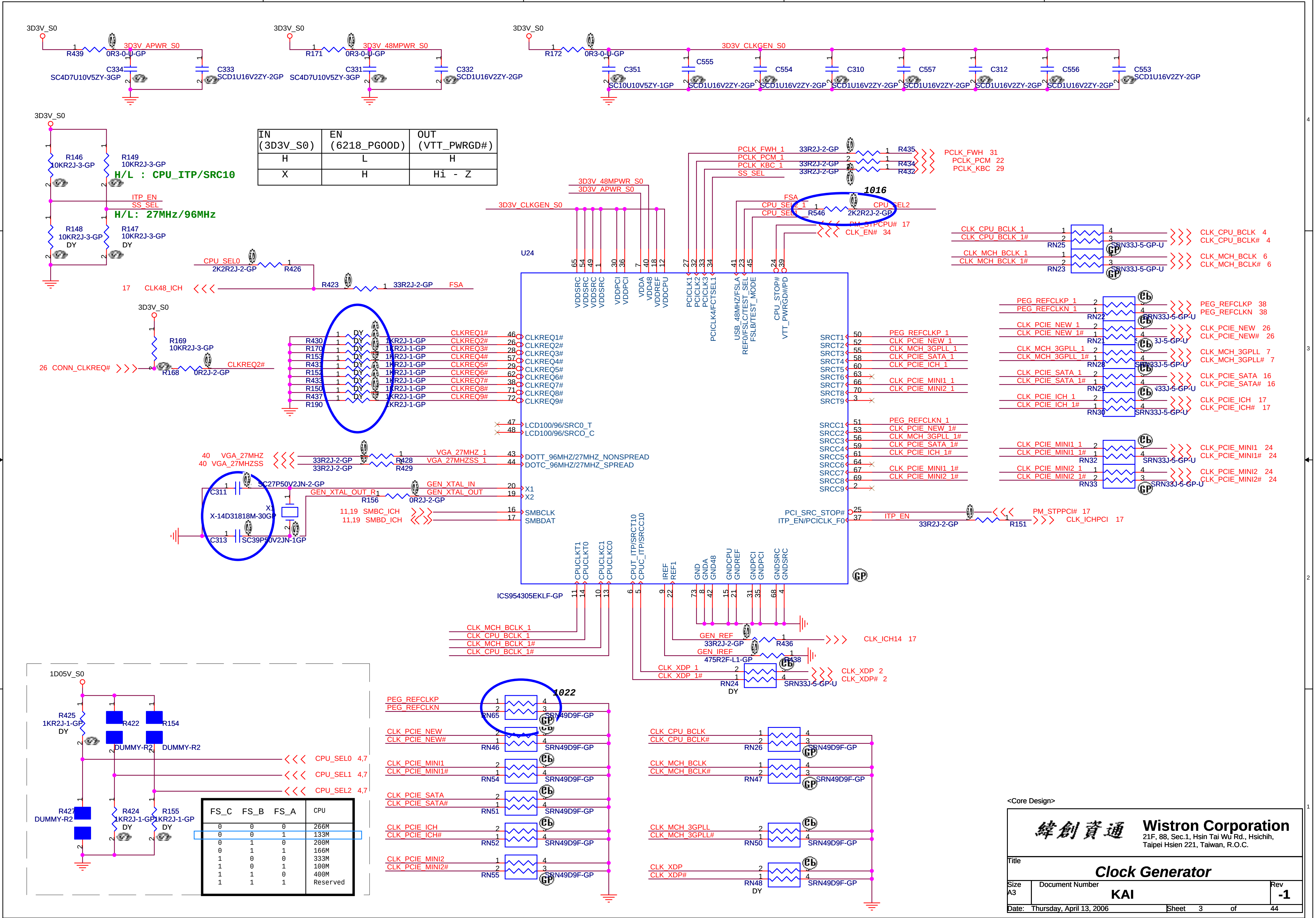
Title	ITP	
Size A3	Document Number KAI	Rev -1
Date: Thursday, April 13, 2006	Sheet 2 of 44	



IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

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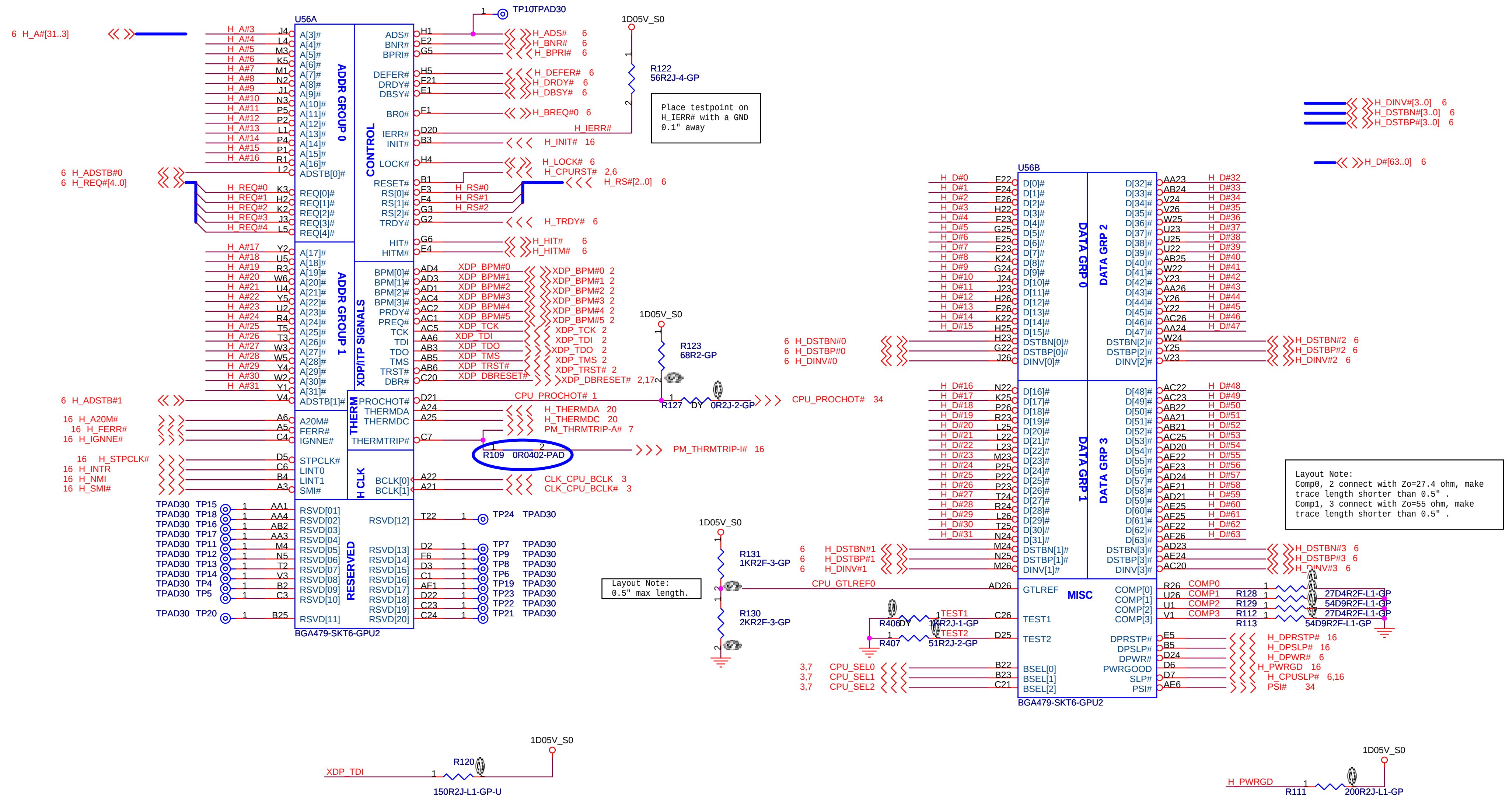
Title: **Clock Generator**

Size	Document Number	Rev
A3	KAI	-1

Date: Thursday, April 13, 2006 Sheet 3 of 44



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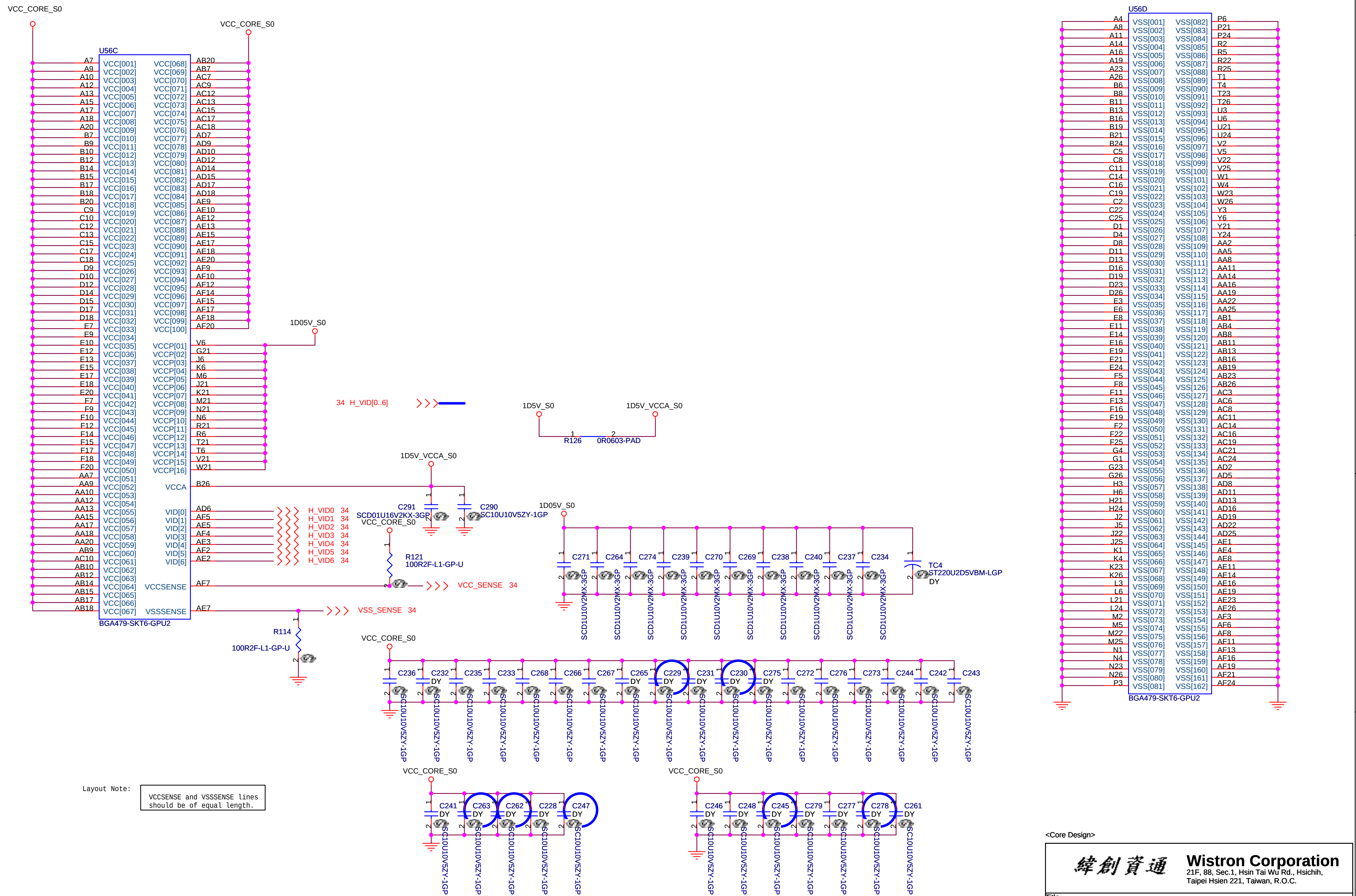
Title	*CPU (1 of 2)*	
Size A3	Document Number KAI	Rev -1
Date: Thursday, April 13, 2006	Sheet 4 of 44	



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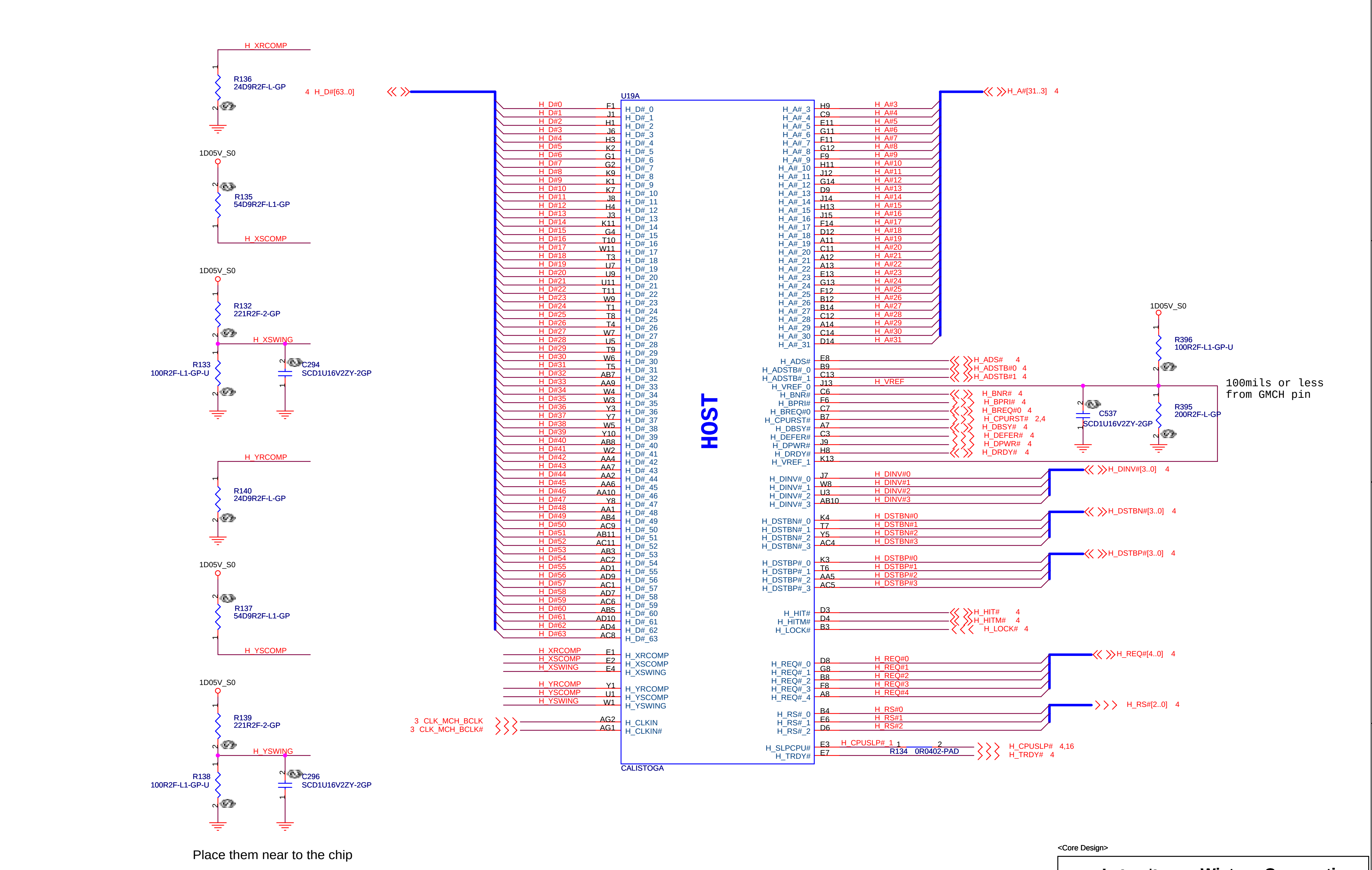
Title		
CPU (2 of 2)		
Size: A3	Document Number: KAI	Rev: -1
Date: Thursday, April 13, 2006	Sheet 5 of 44	



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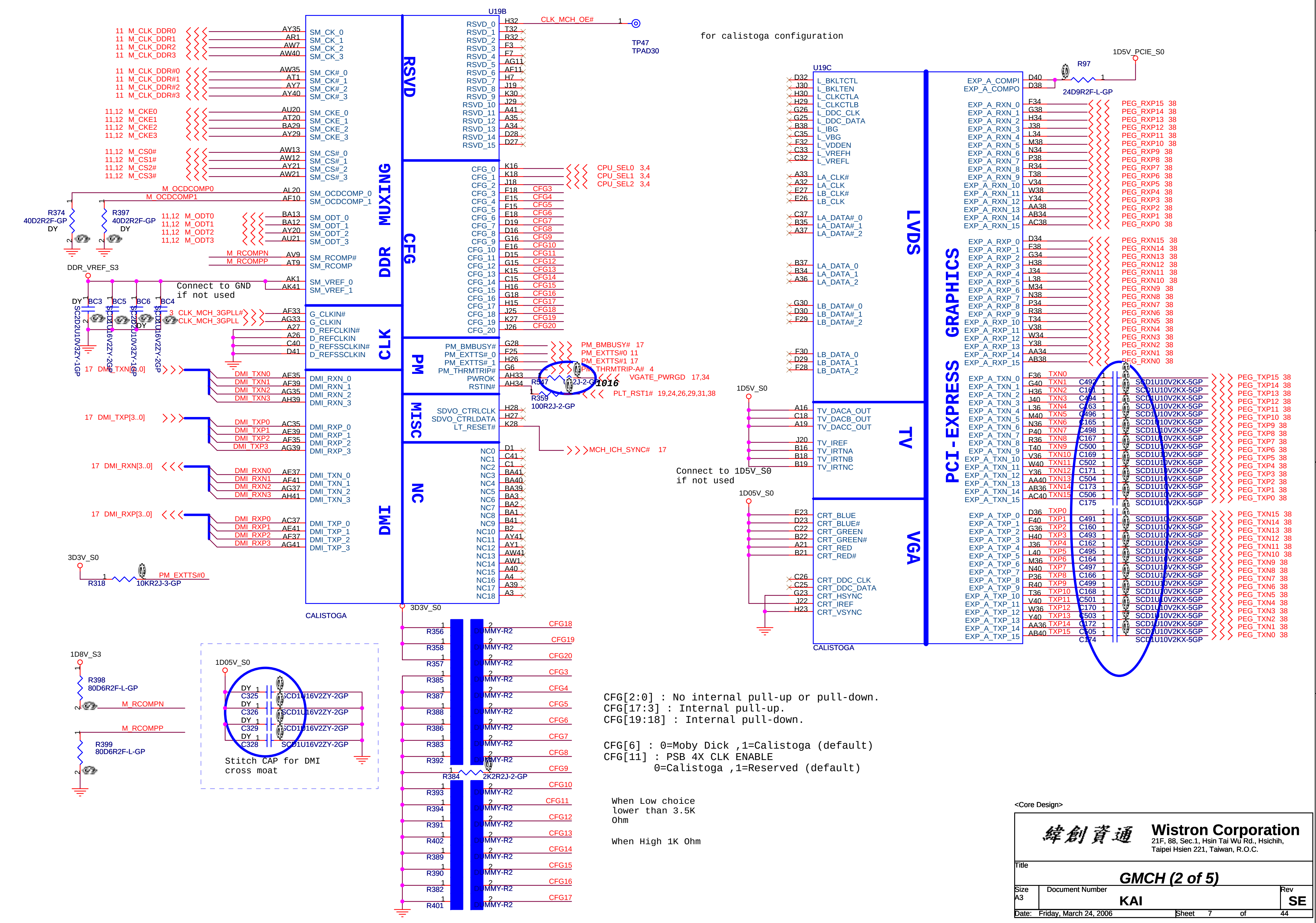
Title: **GMCH (1 of 5)**

Size	Document Number	Rev
A3	KAI	-1

Date: Thursday, April 13, 2006 Sheet 6 of 44



CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-up.
CFG[19:18] : Internal pull-down.

CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
0=Calistoga ,1=Reserved (default)

When Low choice
lower than 3.5K
Ohm

When High 1K Ohm

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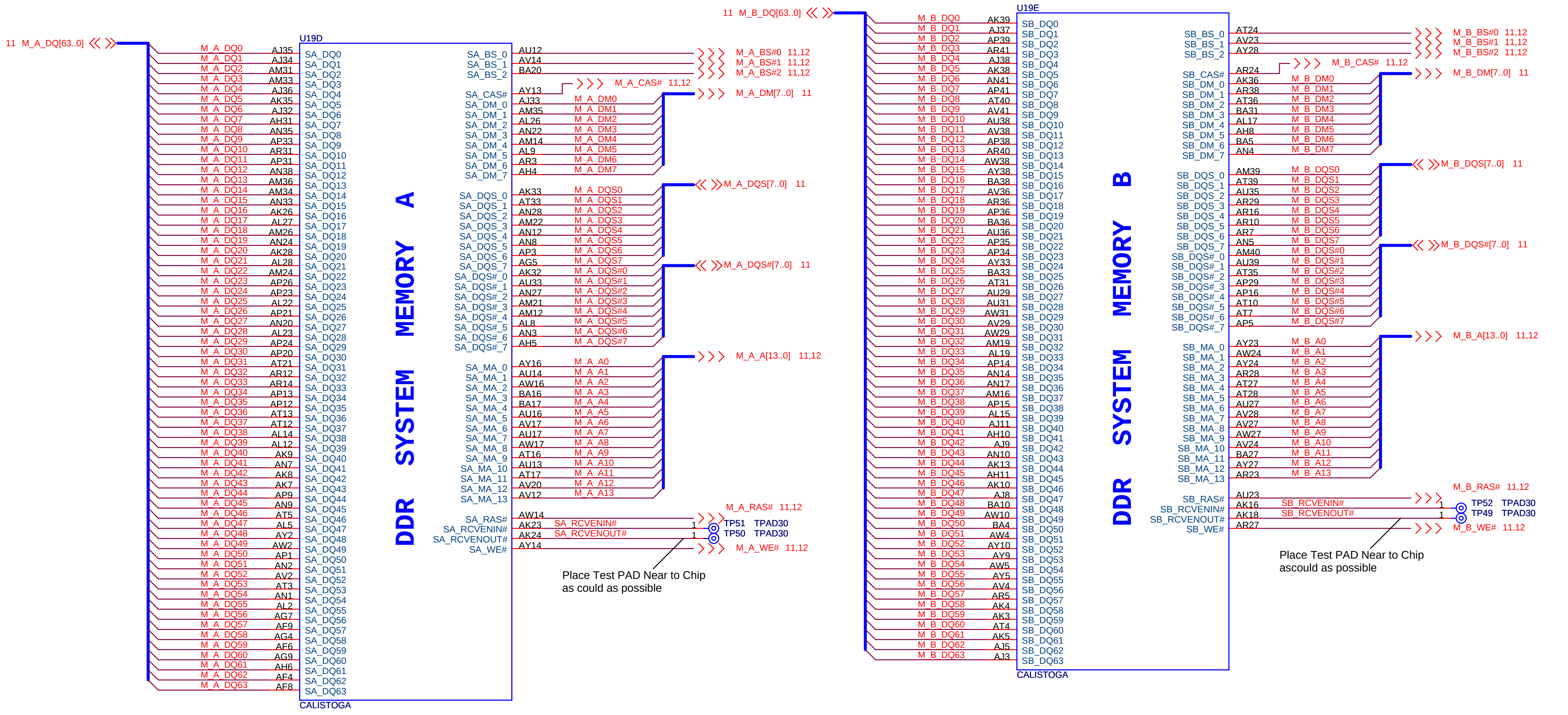
Title		
GMCH (2 of 5)		
Size A3	Document Number KAI	Rev SE
Date: Friday, March 24, 2006	Sheet 7 of 44	



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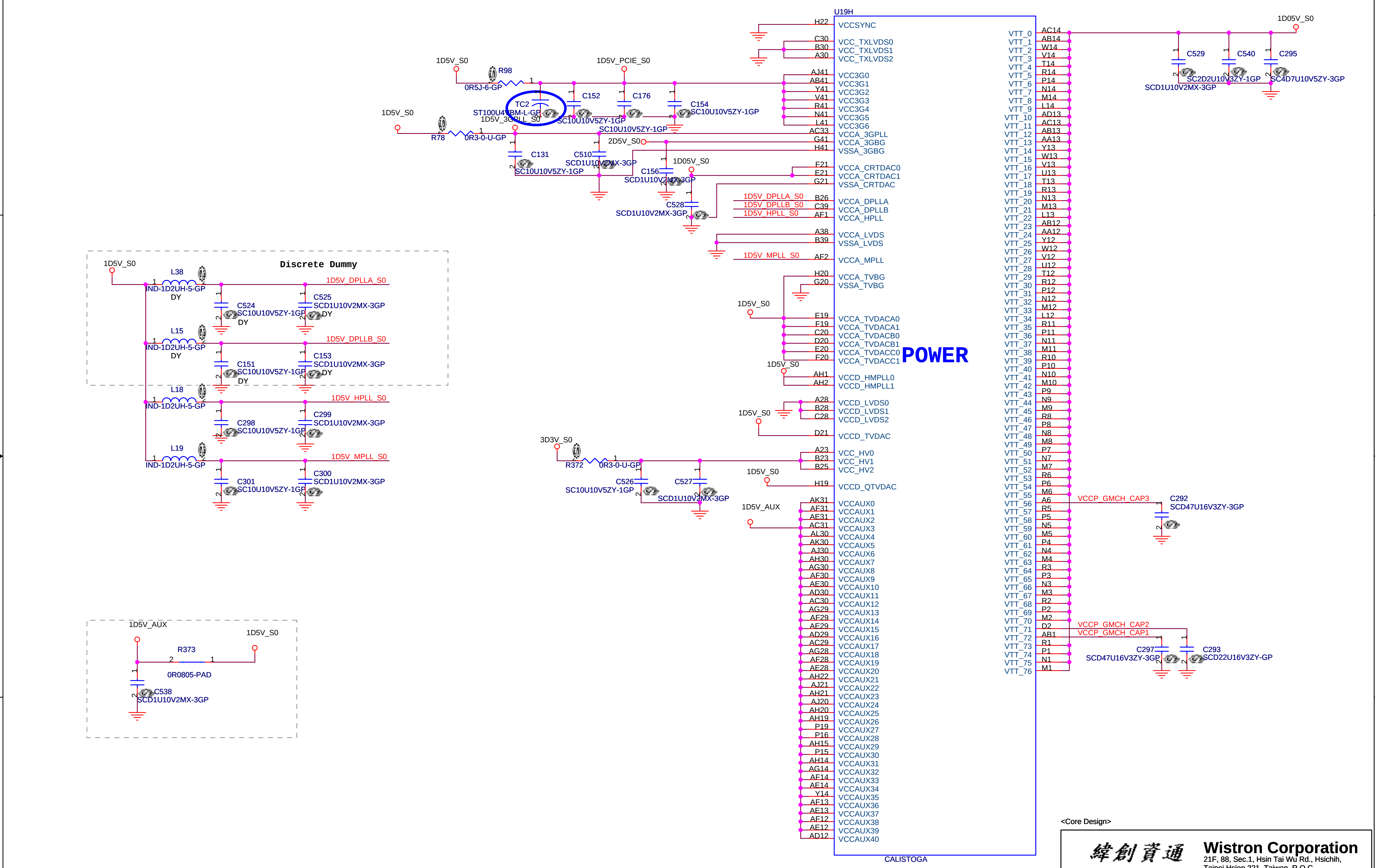
Title	GMCH (3 of 5)	
Size A3	Document Number KAI	Rev SE
Date: Friday, March 24, 2006	Sheet 8 of 44	



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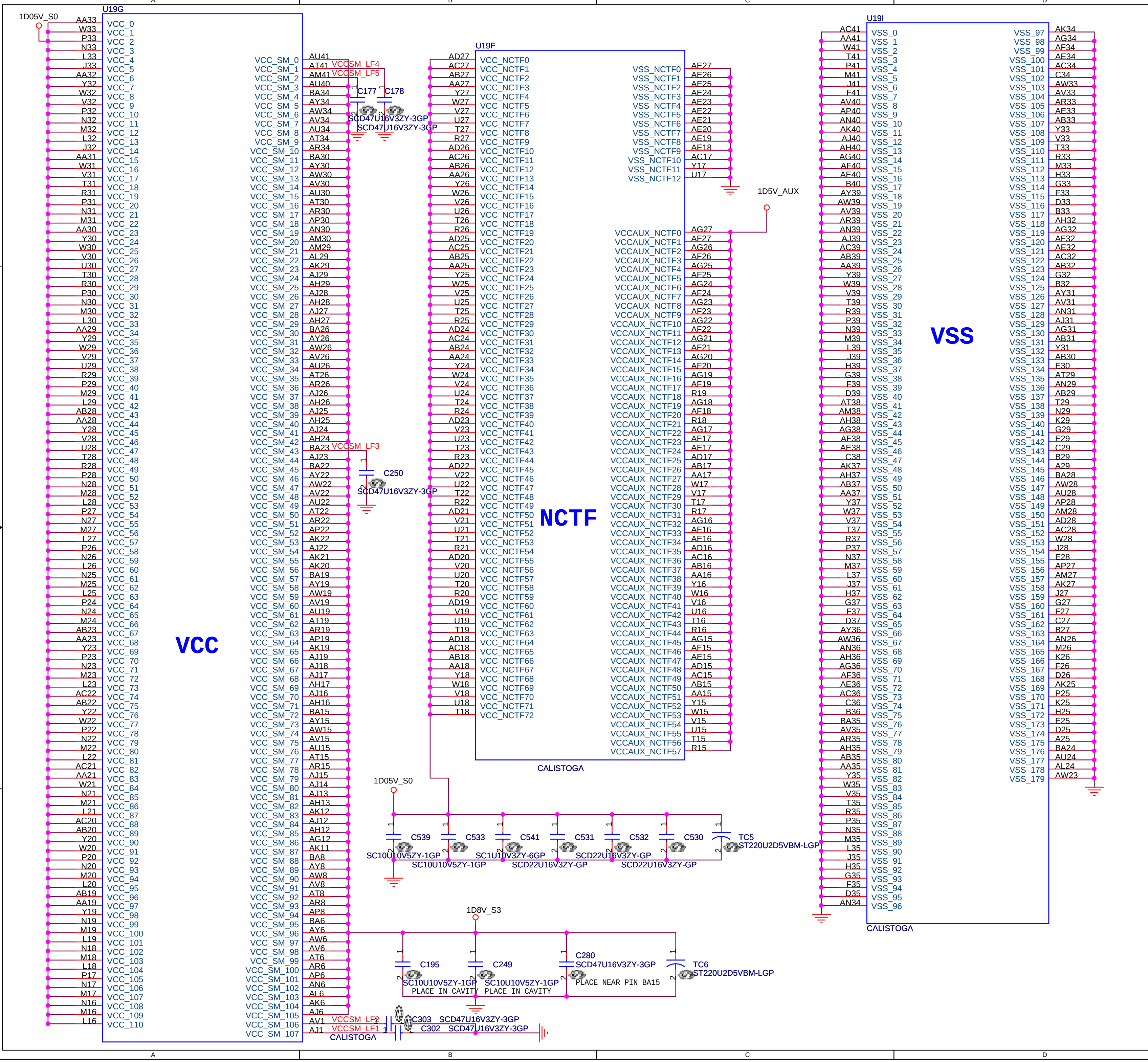
Title		
GMCH (4 of 5)		
Size: A3	Document Number: KAI	Rev: SE
Date: Friday, March 24, 2006	Sheet 9 of 44	



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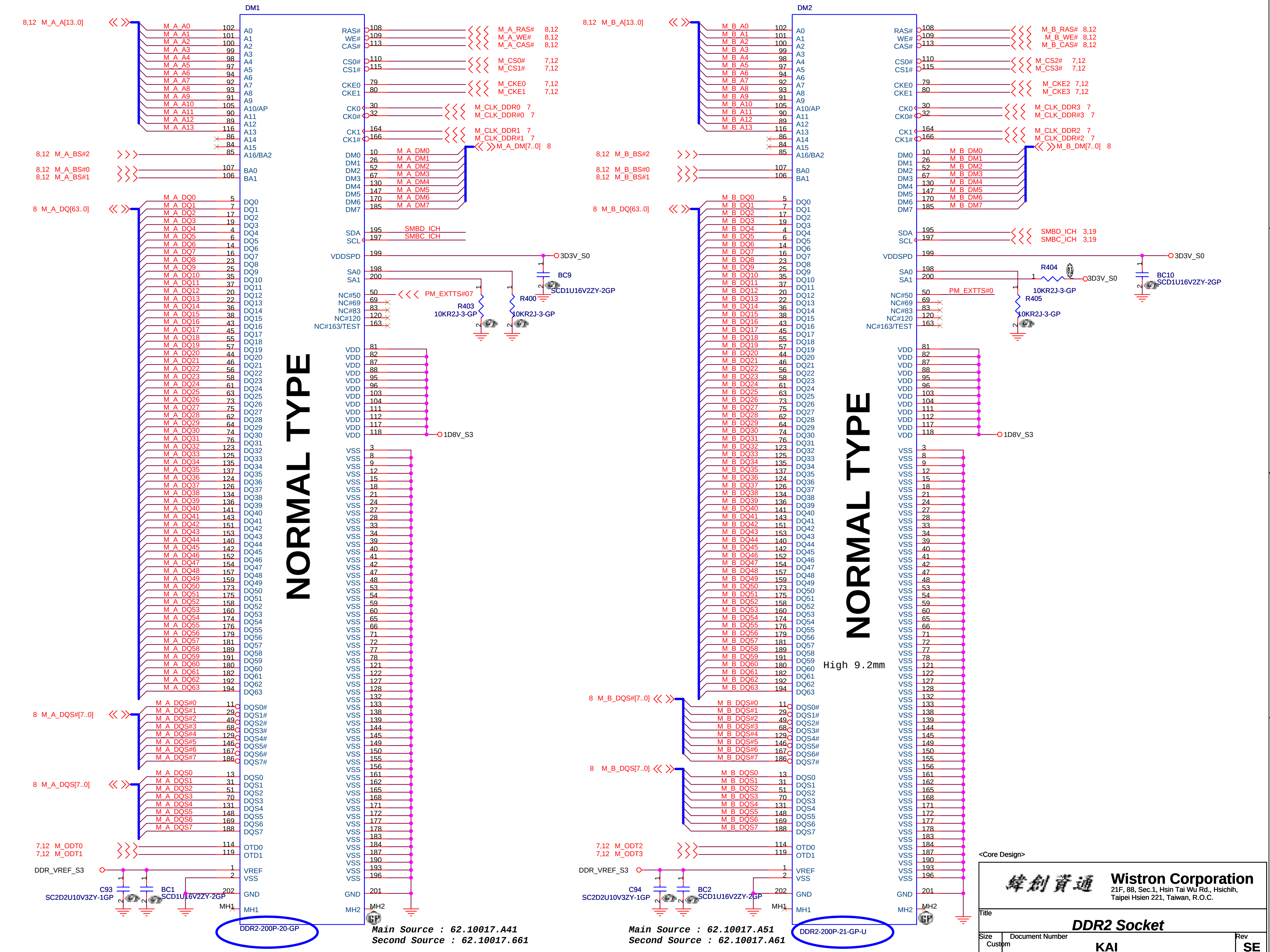
Title: **GMCH (5 of 5)**

Size: A3 | Document Number: KAI | Rev: SE

Date: Friday, March 24, 2006 | Sheet 10 of 44



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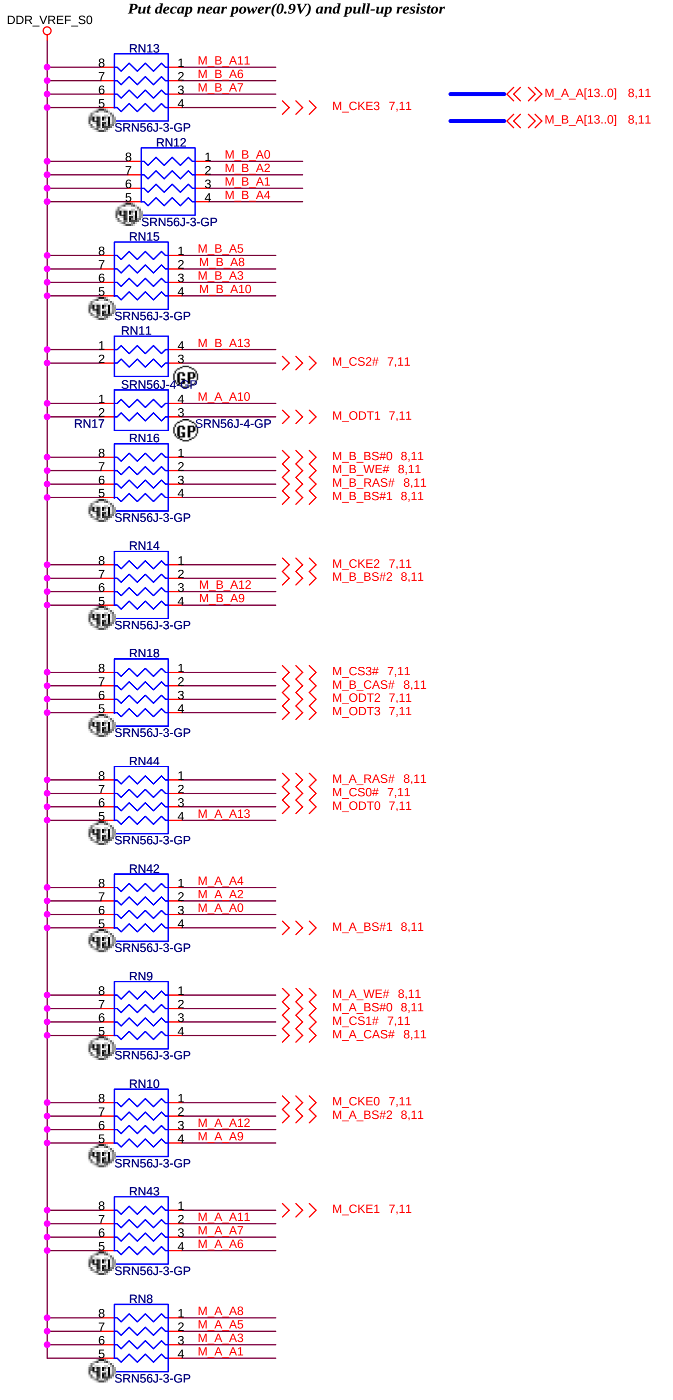
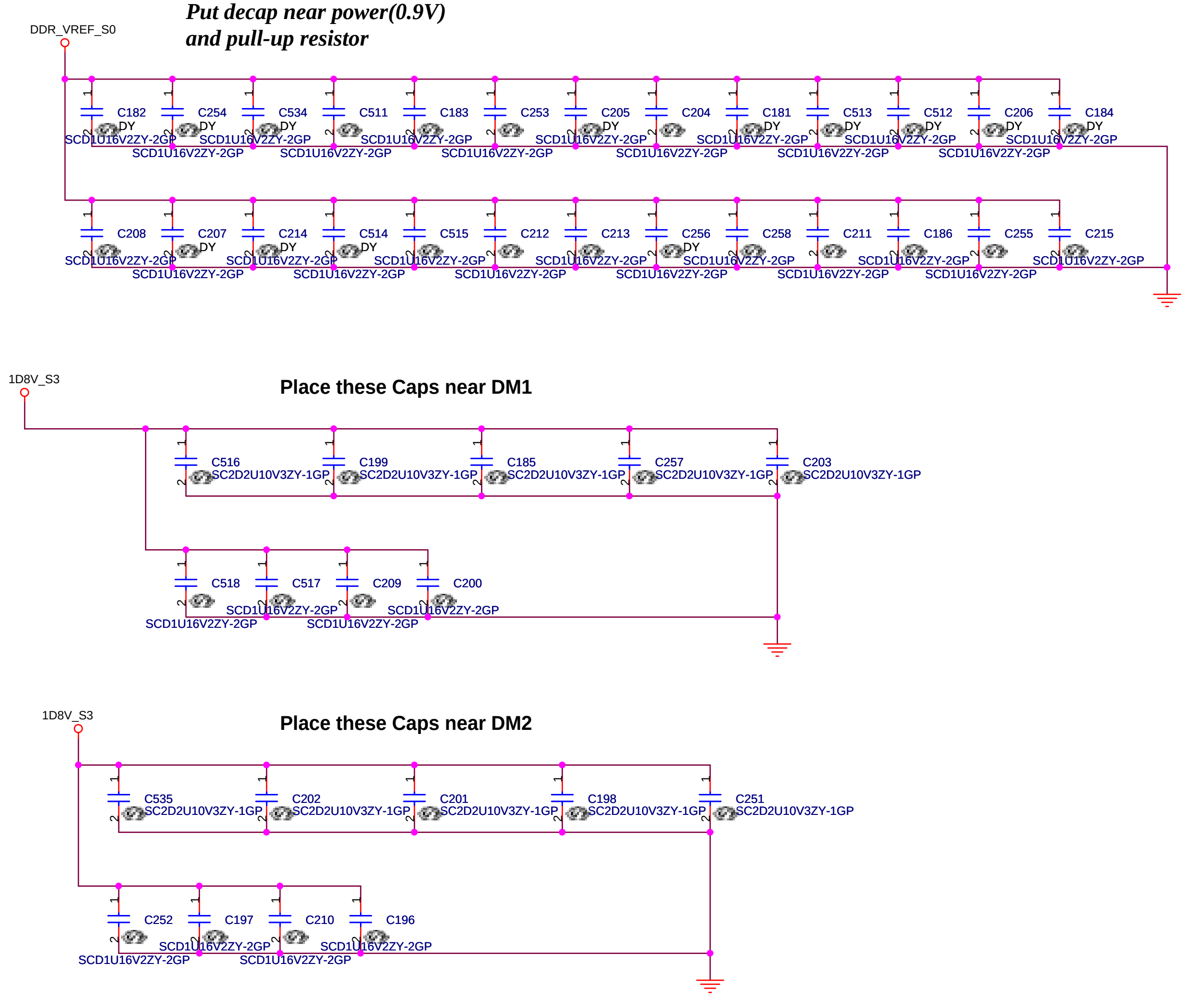
Title	**DDR2 Socket**	
Size: Custom	Document Number: KAI	Rev: SE
Date: Thursday, April 13, 2006	Sheet 11 of 44	

PARALLEL TERMINATION



Decoupling Capacitor



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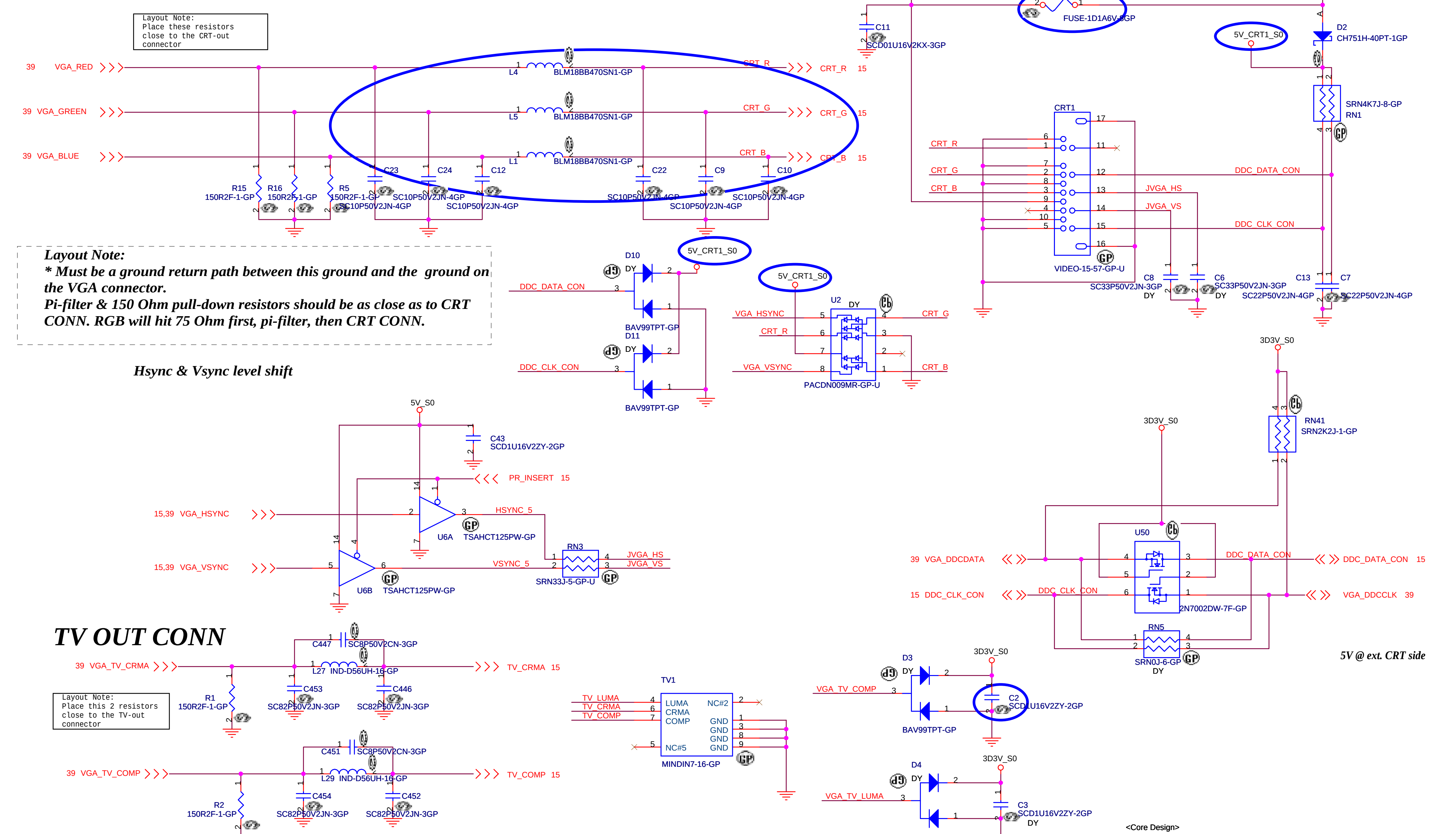
Title: DDR2 Termination Resistor		
Size: A3	Document Number: KAI	Rev: SE
Date: Friday, March 24, 2006	Sheet 12 of 44	

CRT I/F & CONNECTOR



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緯創資通 **Wistron Corporation**
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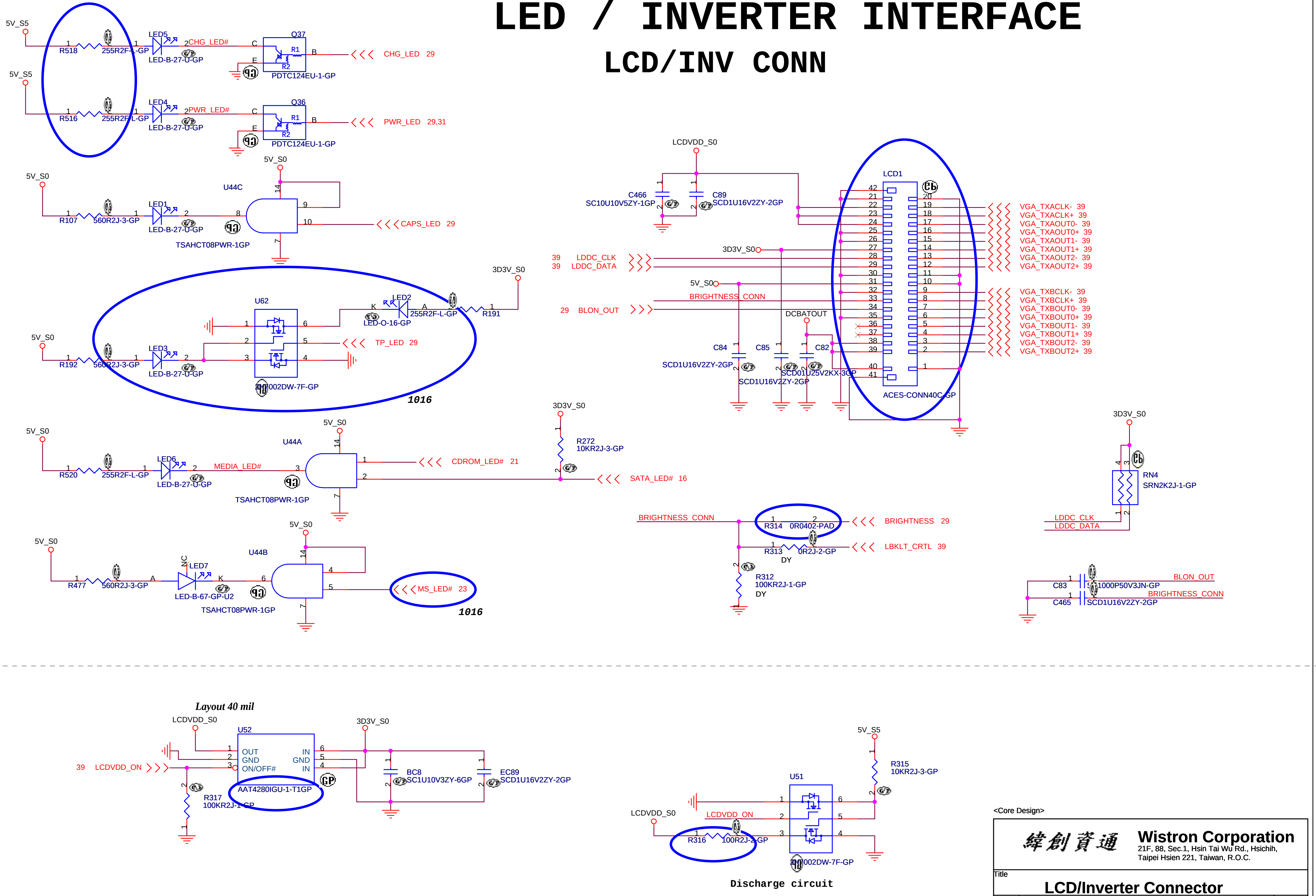
Title	CRT/TV Connector	
Size A3	Document Number KAI	Rev SE
Date: Wednesday, March 29, 2006	Sheet 13 of 44	

LED / INVERTER INTERFACE

LCD/INV CONN



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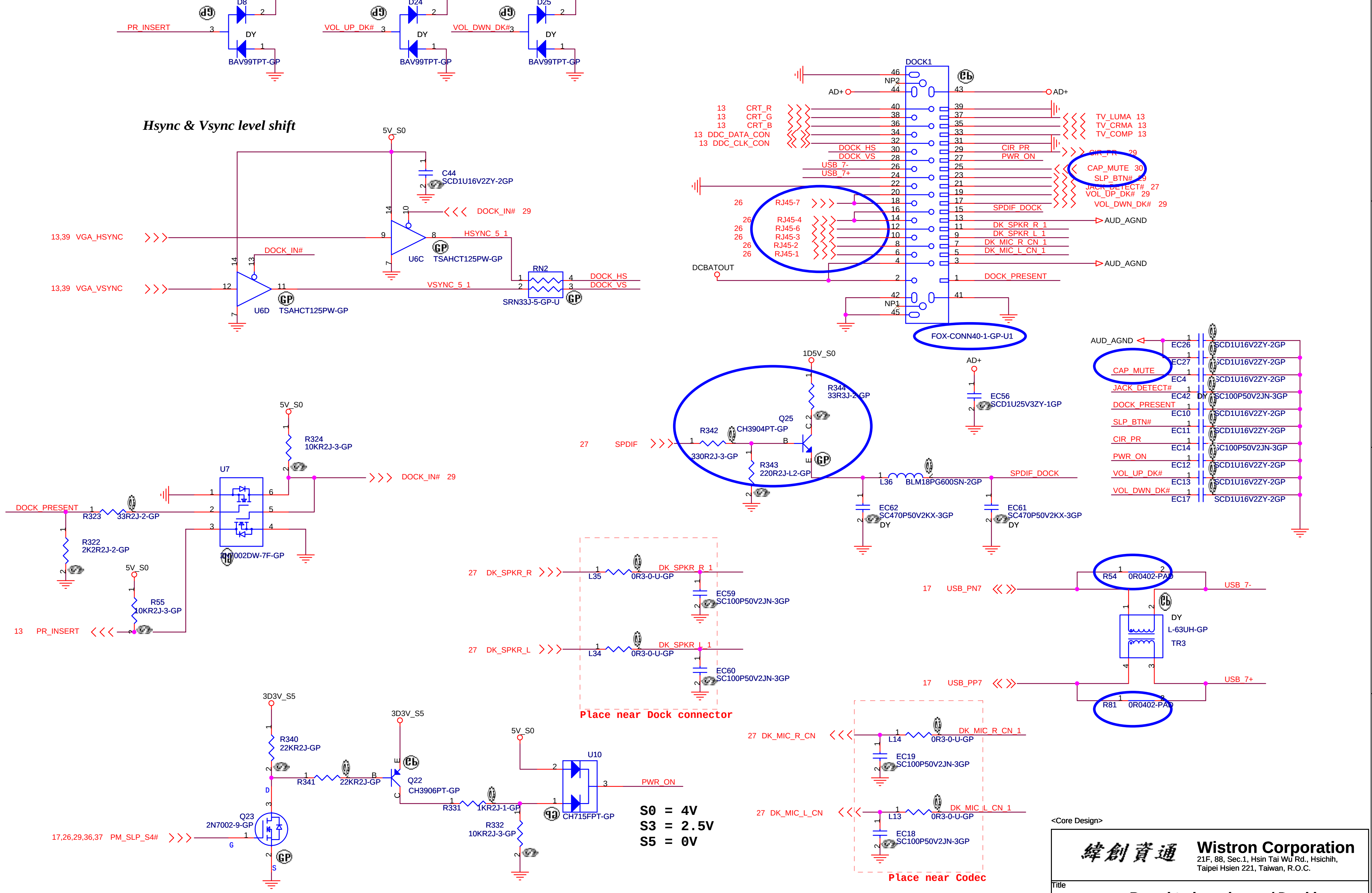
Title	LCD/Inverter Connector		
Size: Custom	Document Number: KAI		Rev: SE
Date: Thursday, April 13, 2006	Sheet 14	of 44	

Docking Connector



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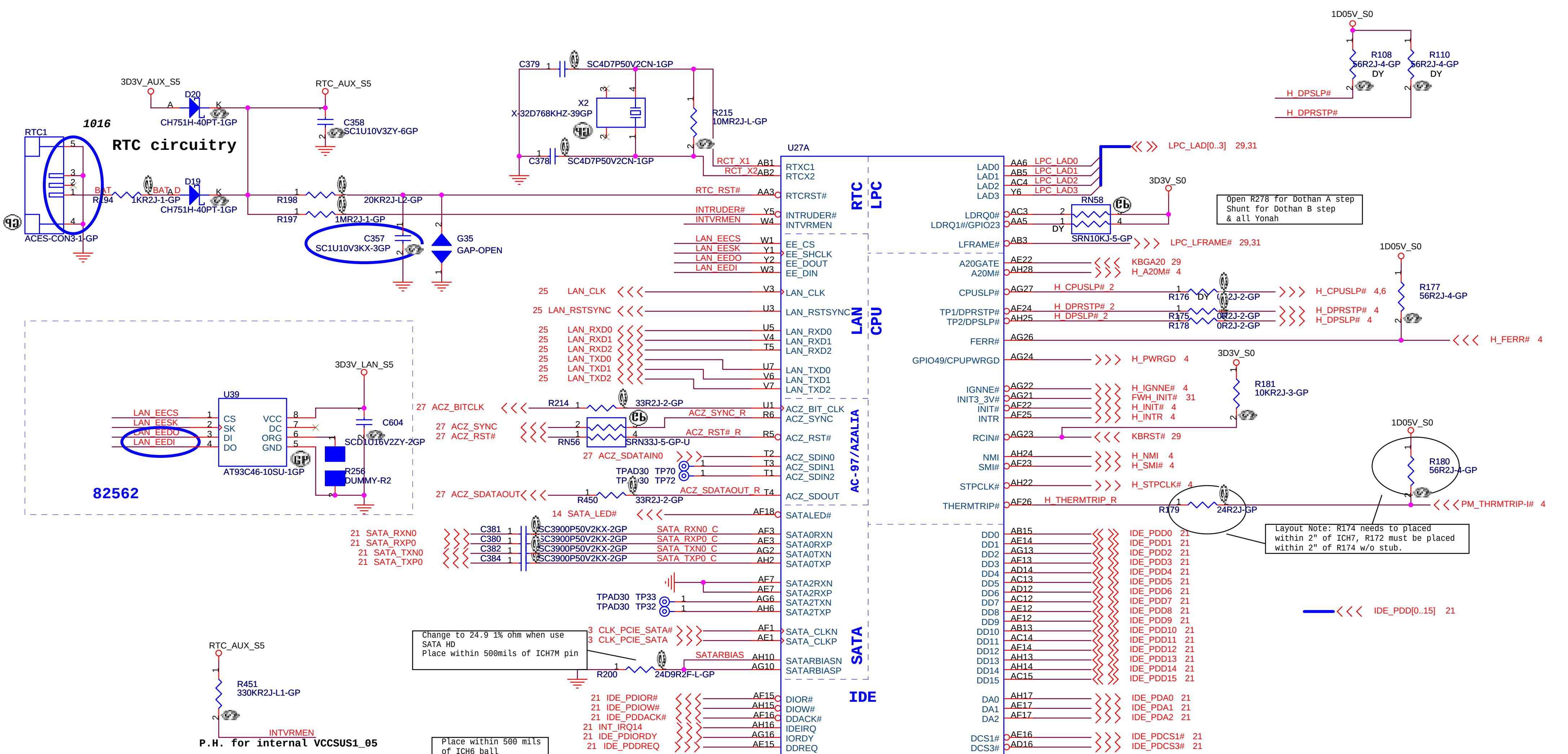
Title: **Board to board conn/ Docking**

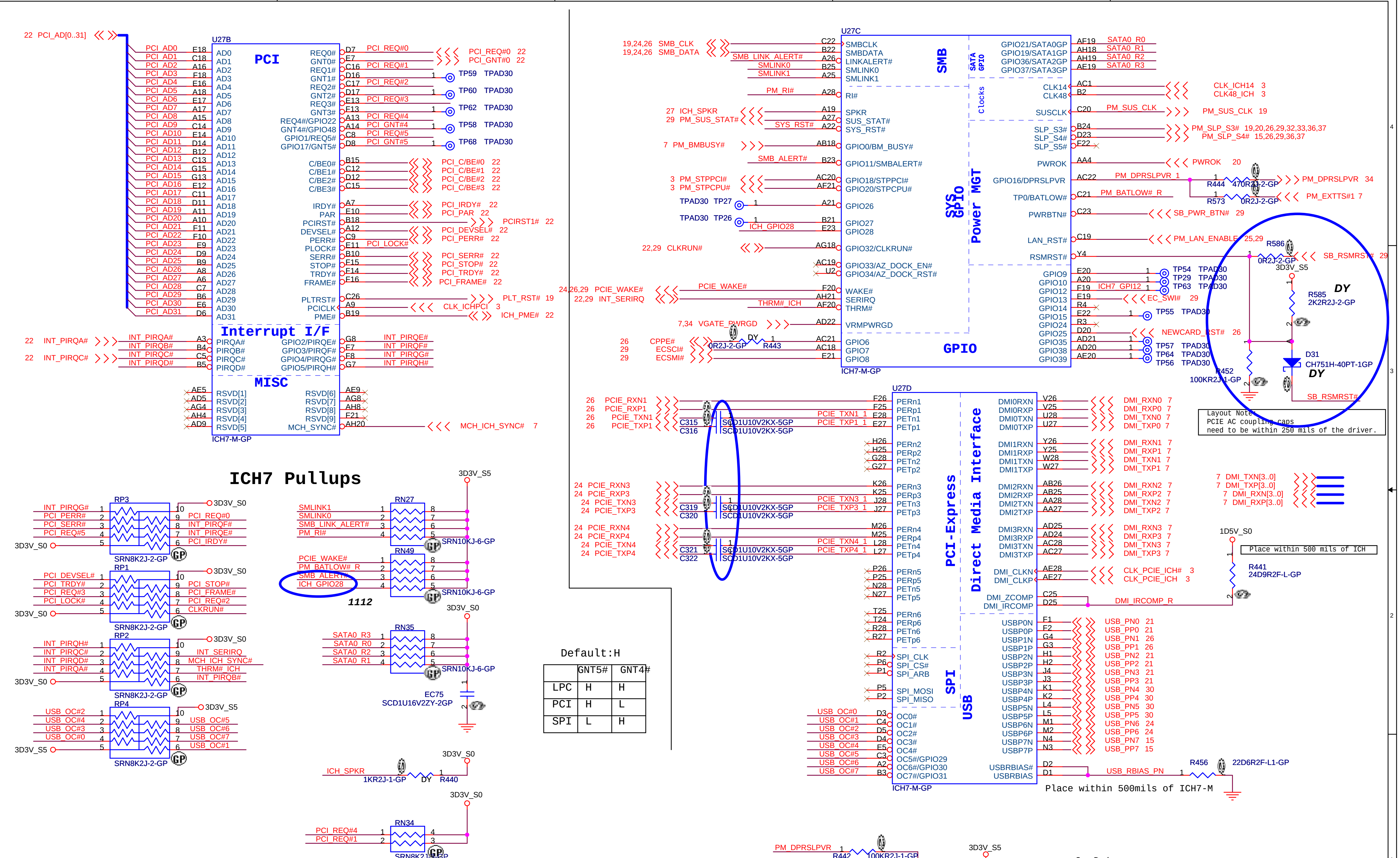
Size	Document Number	Rev
A3	KAI	SE

Date: Sunday, May 28, 2006 Sheet 15 of 44



	INTVRMEN
Enable	1
Disable	0

Placement Note:
Diatance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.



Default:H

	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H

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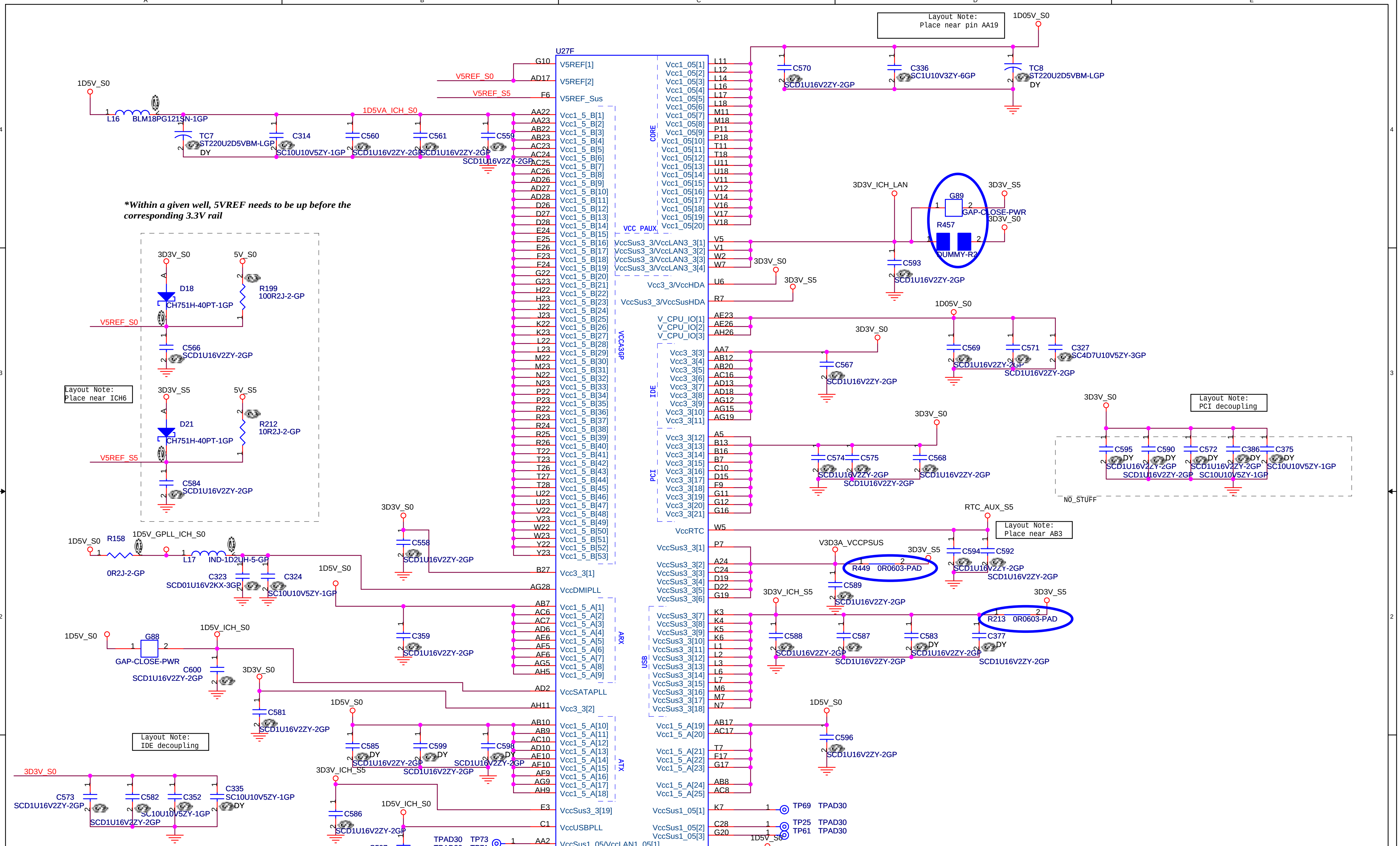
Title		
ICH7-M (2 of 4)		
Size A3	Document Number KAI	Rev SE
Date: Thursday, April 13, 2006	Sheet 17 of 44	



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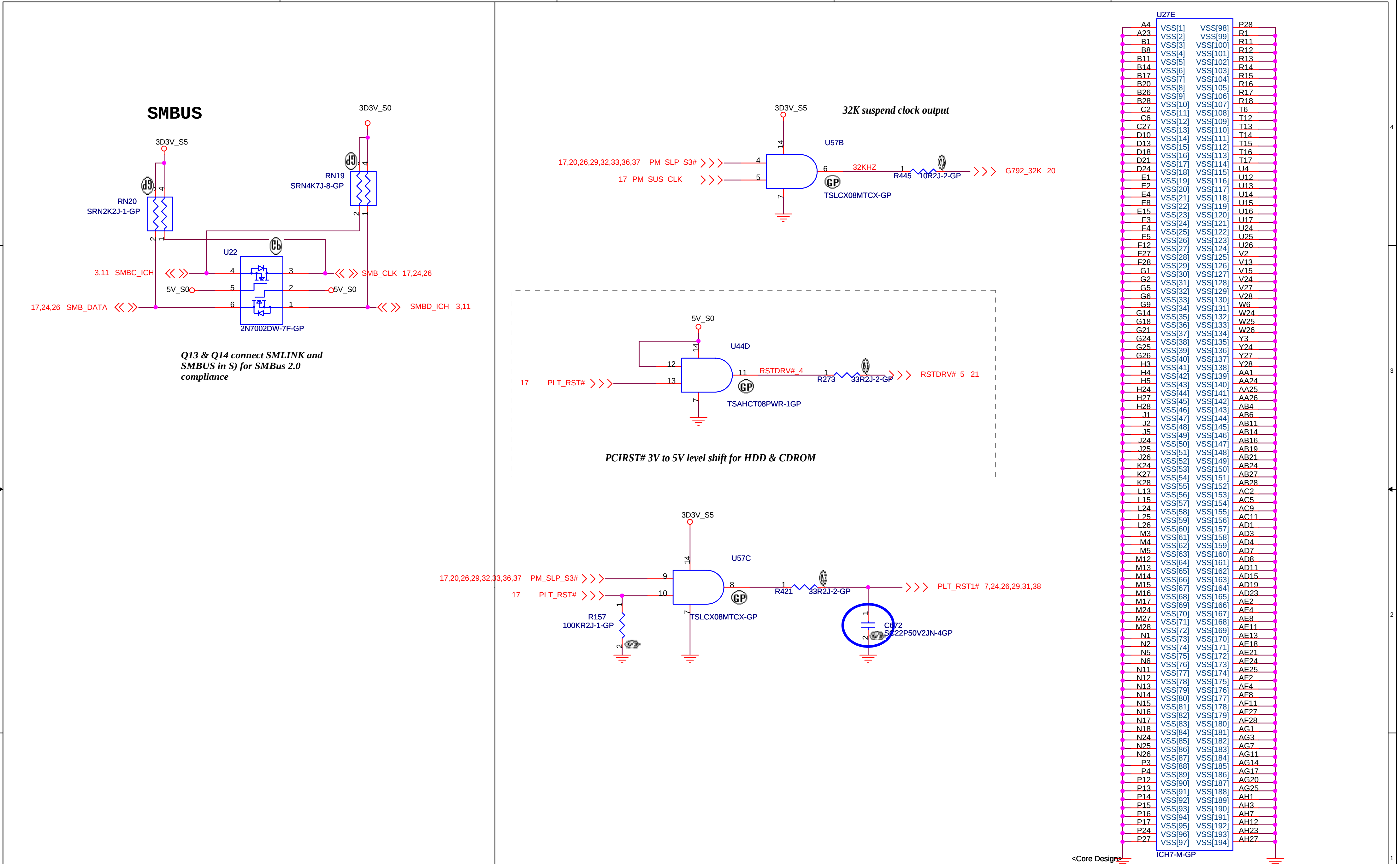
Title	ICH7-M (3 of 4)	
Size A3	Document Number KAI	Rev SE
Date: Friday, March 24, 2006	Sheet 18 of 44	



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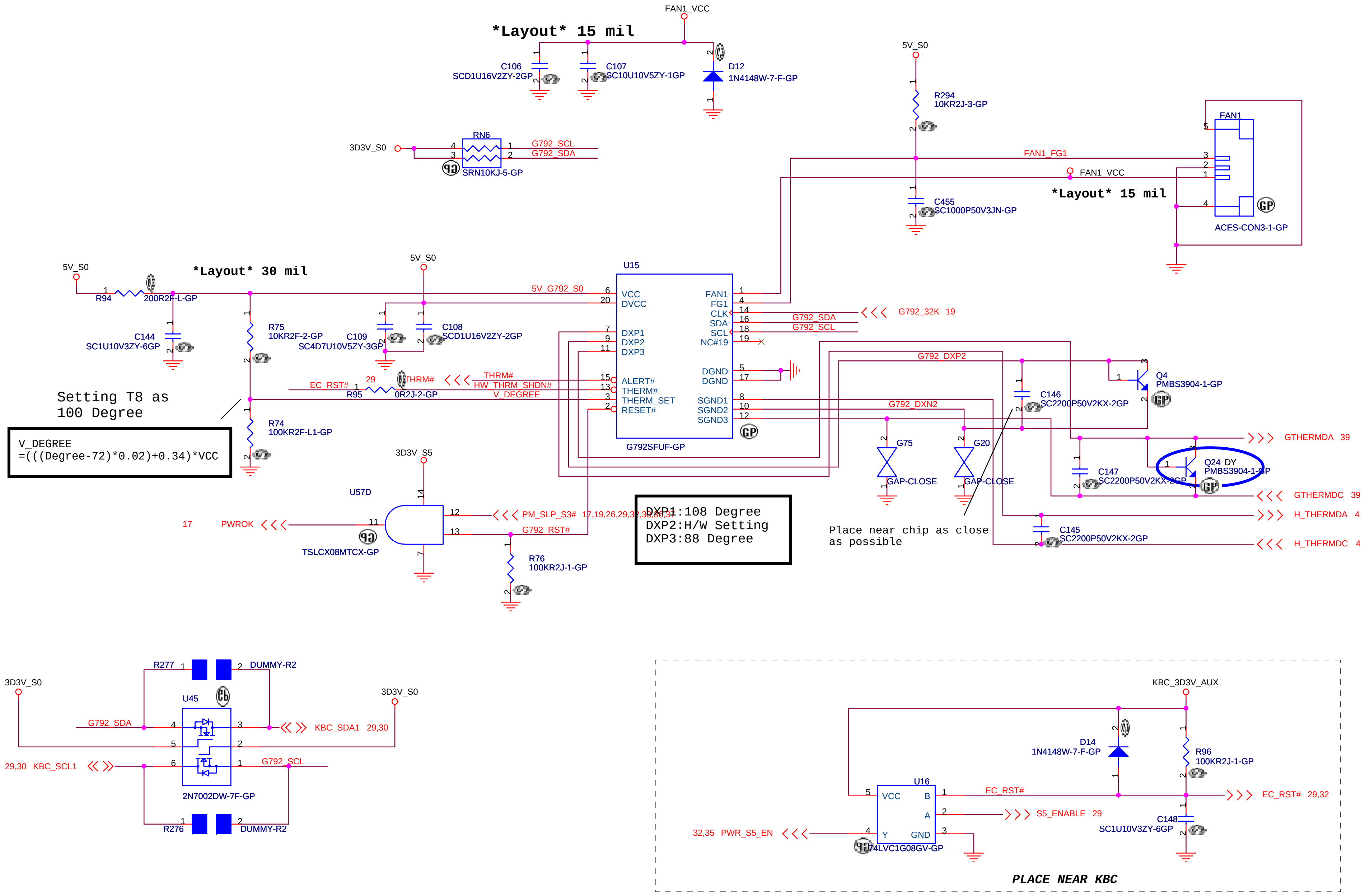
Title		
ICH7-M (4 of 4)		
Size A3	Document Number KAI	Rev SE
Date: Friday, March 24, 2006	Sheet 19 of 44	



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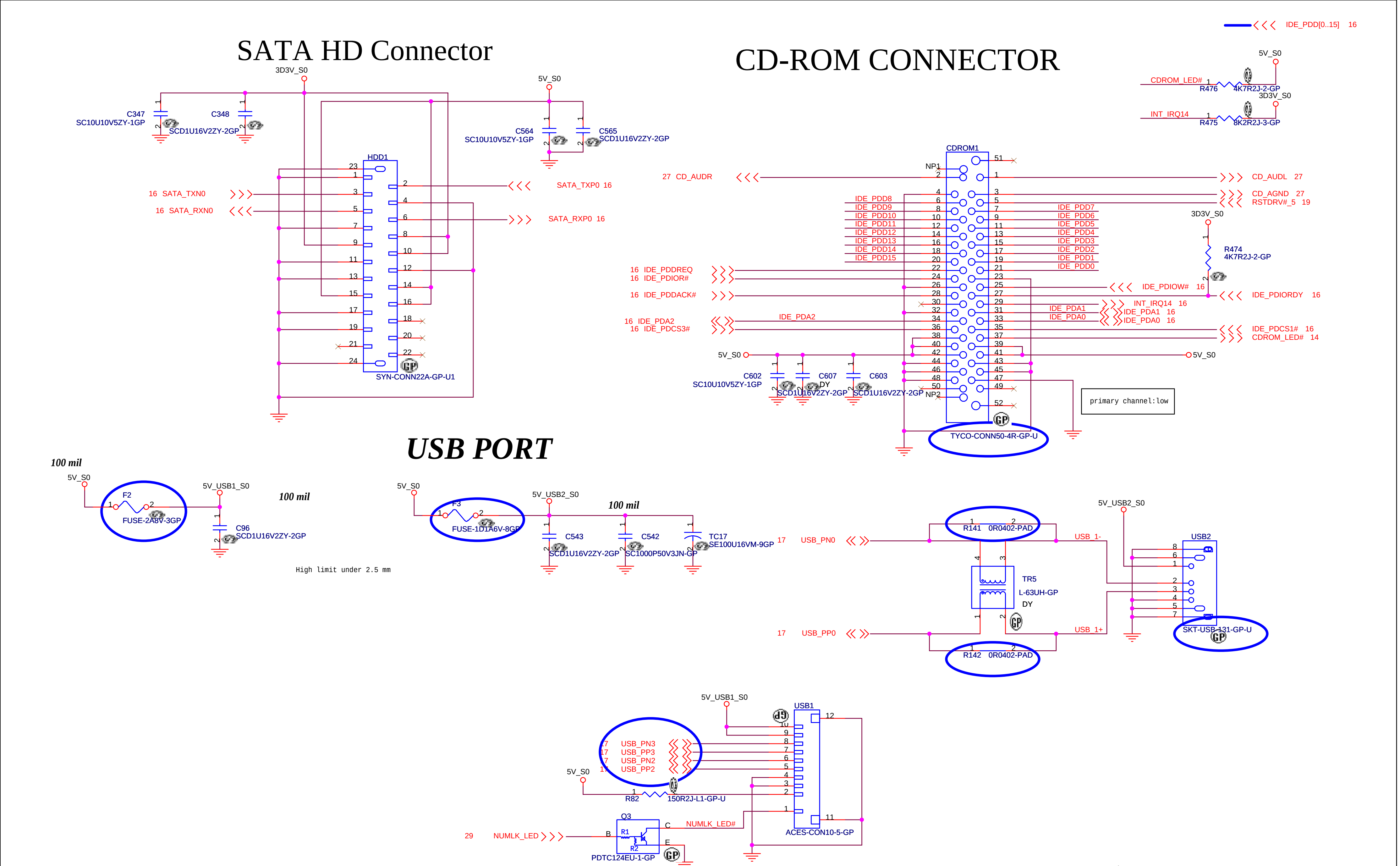
Title
Thermal/Fan Controllor

Size	Document Number	Rev
Custom	KAI	SE

Date: Monday, March 27, 2006 Sheet 20 of 44



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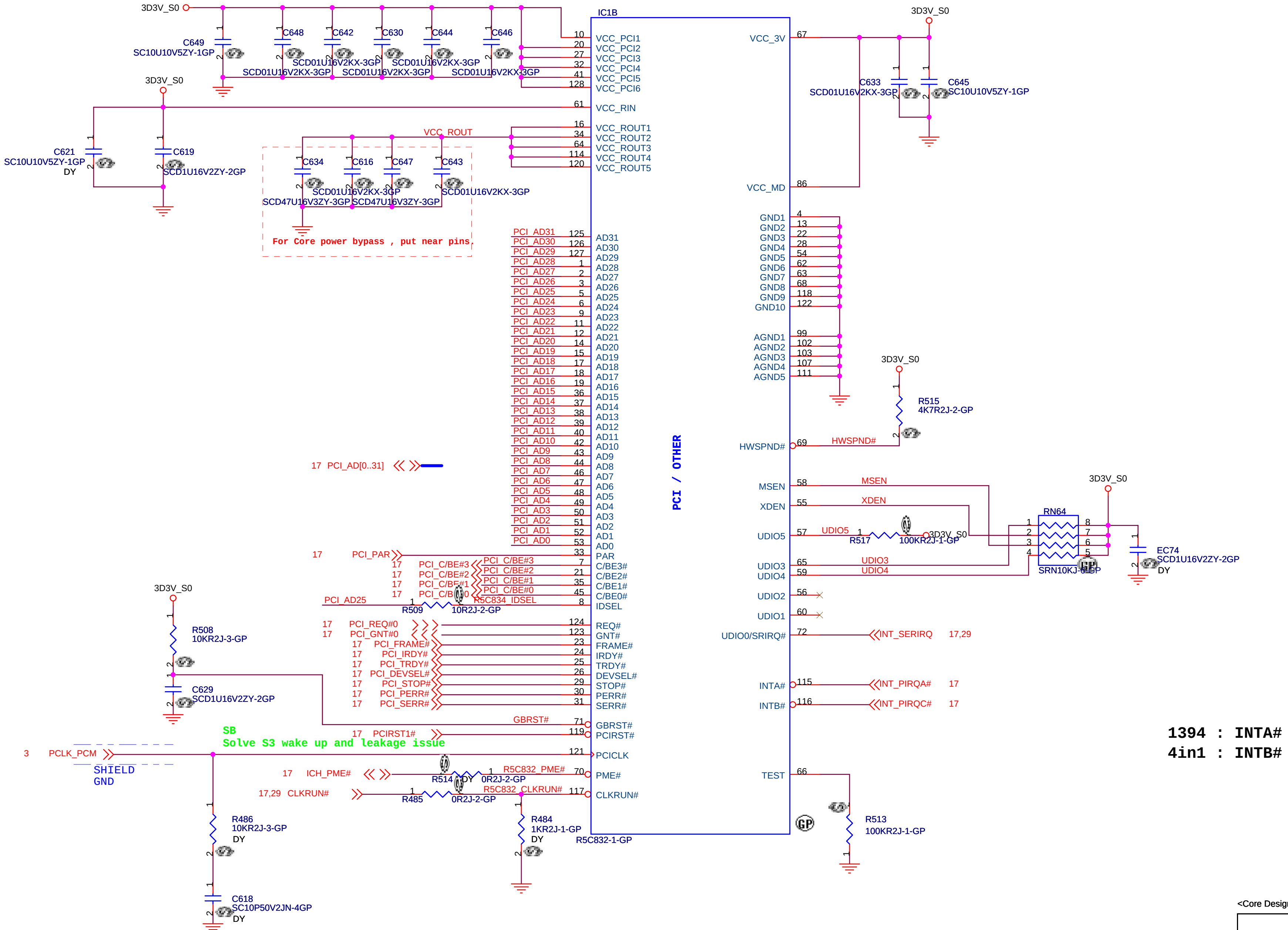
Title	**HD/CDROM**
Size A3	Document Number **KAI** — Rev **SE**
Date: Friday, May 12, 2006	Sheet 21 of 44



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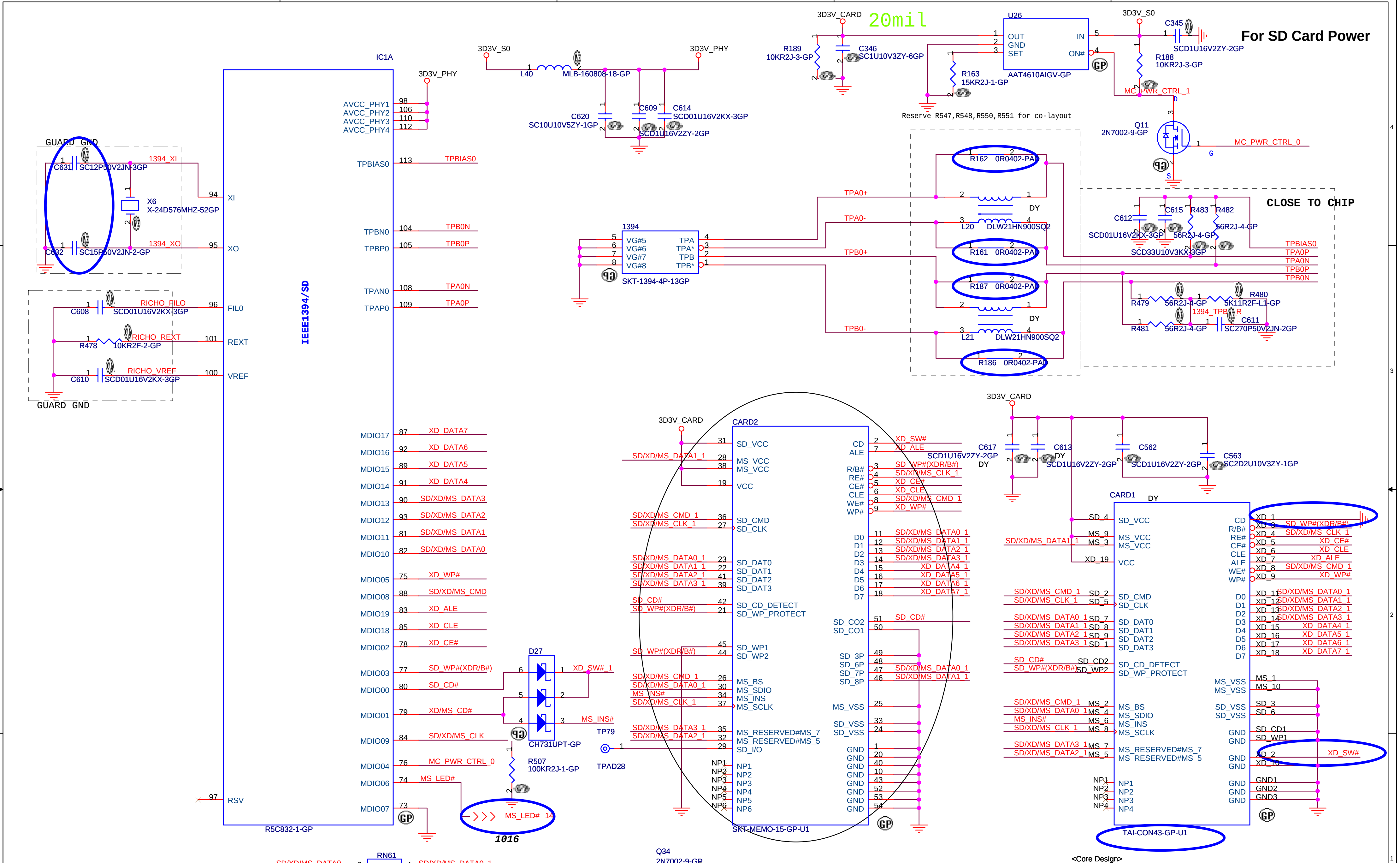
Title	**R5C832/PCI**	
Size A3	Document Number **KAI**	Rev **SE**
Date: Thursday, April 13, 2006	Sheet 22 of 44	



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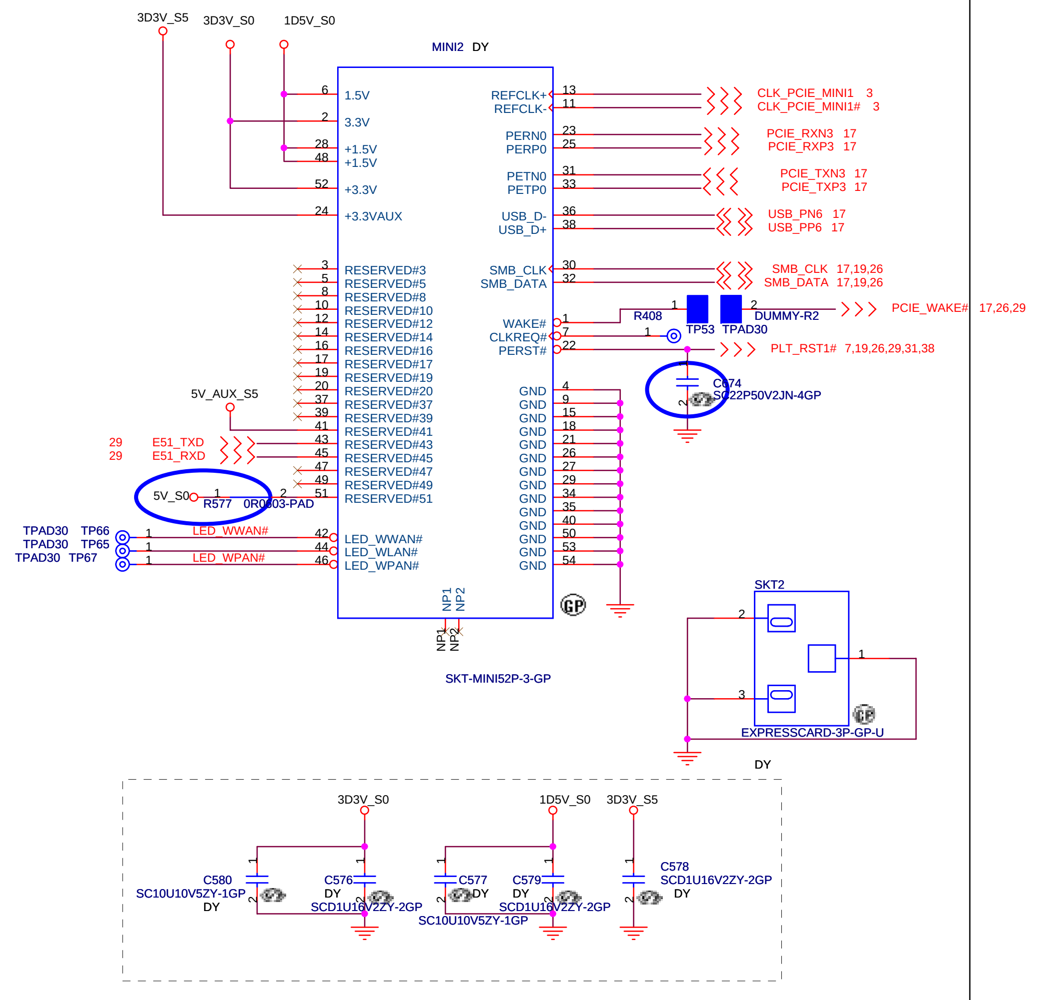
Title: **R5C832/IEEE1394/SD**

Size	Document Number	Rev
A3	KAI	SE

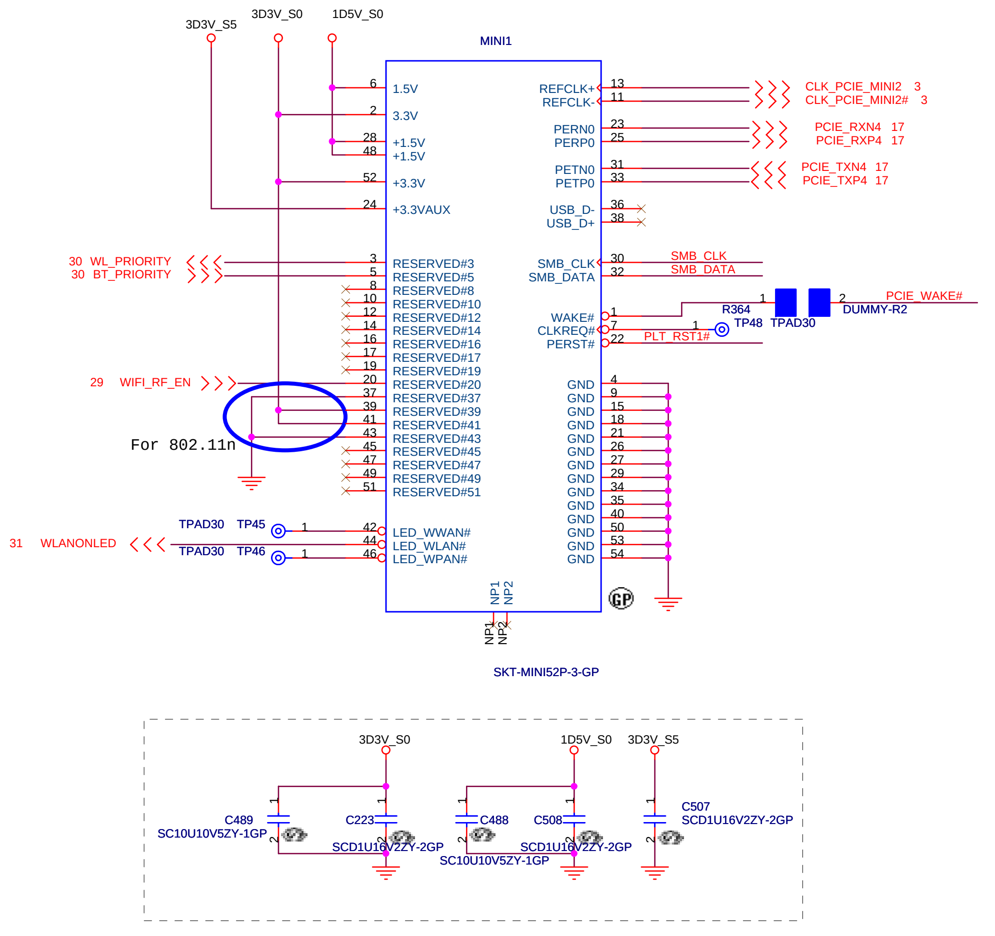
Date: Friday, April 14, 2006 Sheet 23 of 44

Mini Card Connector

Mini Card Connector 2



Mini Card Connector 1



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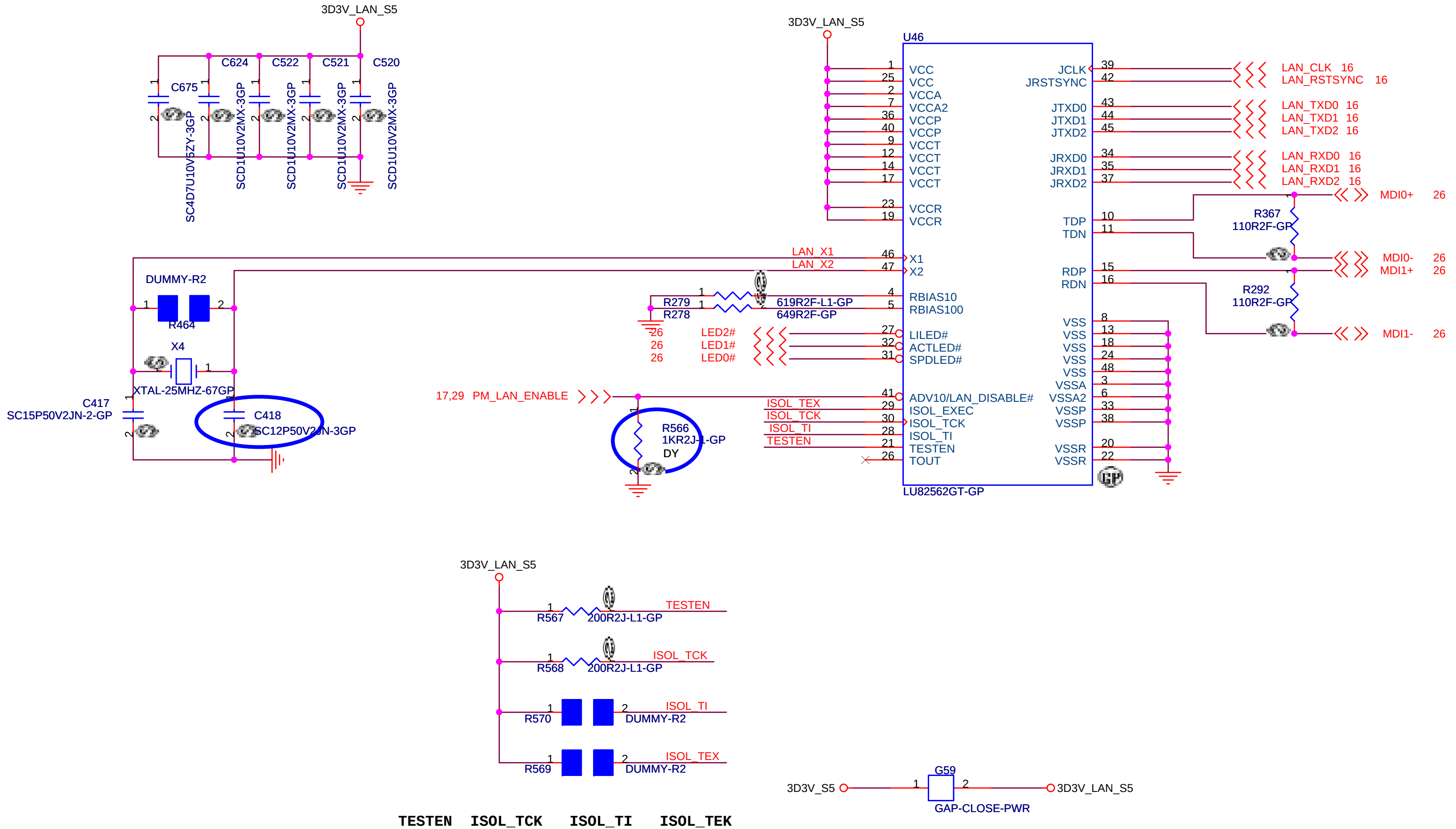
Title	MINI CARD CONN.	
Size A3	Document Number KAI	Rev SE
Date: Wednesday, May 24, 2006	Sheet 24 of 44	



TESTEN	ISOL_TCK	ISOL_TI	ISOL_TEK	
0	0	0	0	MODE0
0	0	1	1	MODE1
1	0	0	1	MODE2
1	0	1	1	MODE3
1	1	0	0	MODE4

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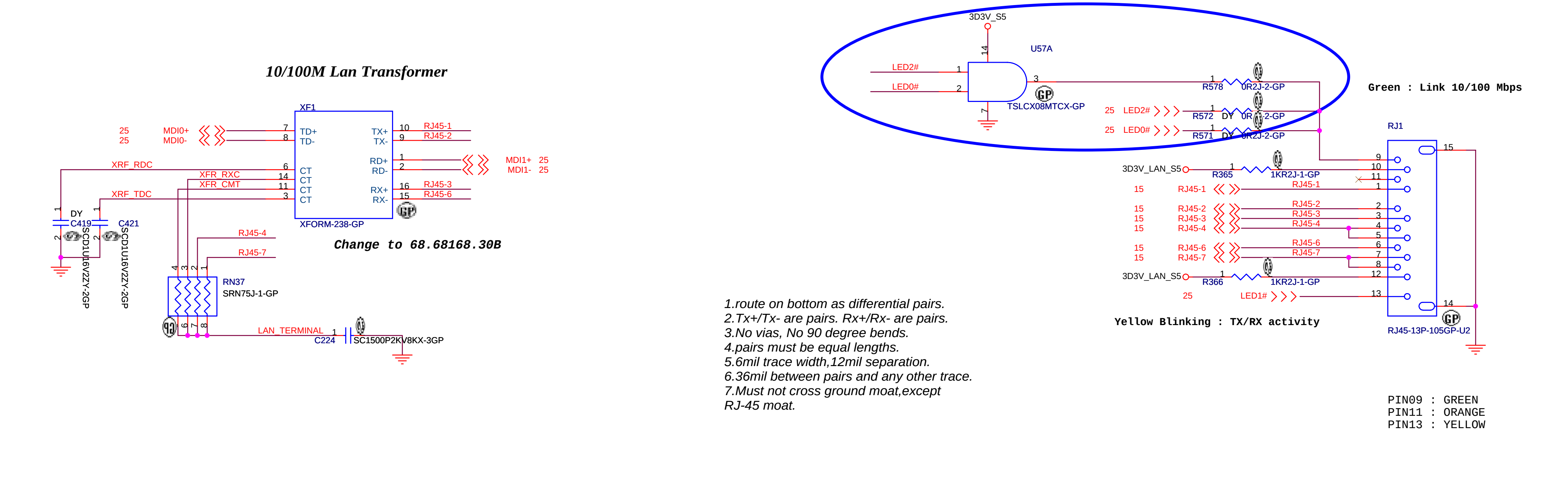
Title: **LAN TEKOA**

Size: A3 | Document Number: KAI | Rev: SE

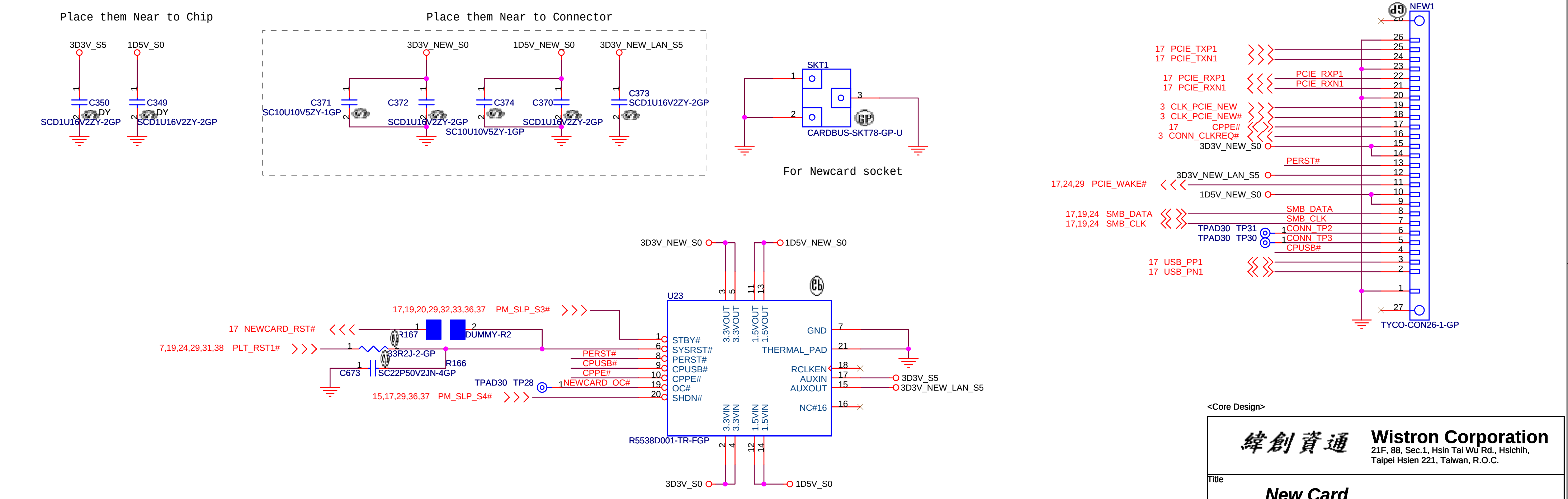
Date: Monday, March 27, 2006 | Sheet 25 of 44

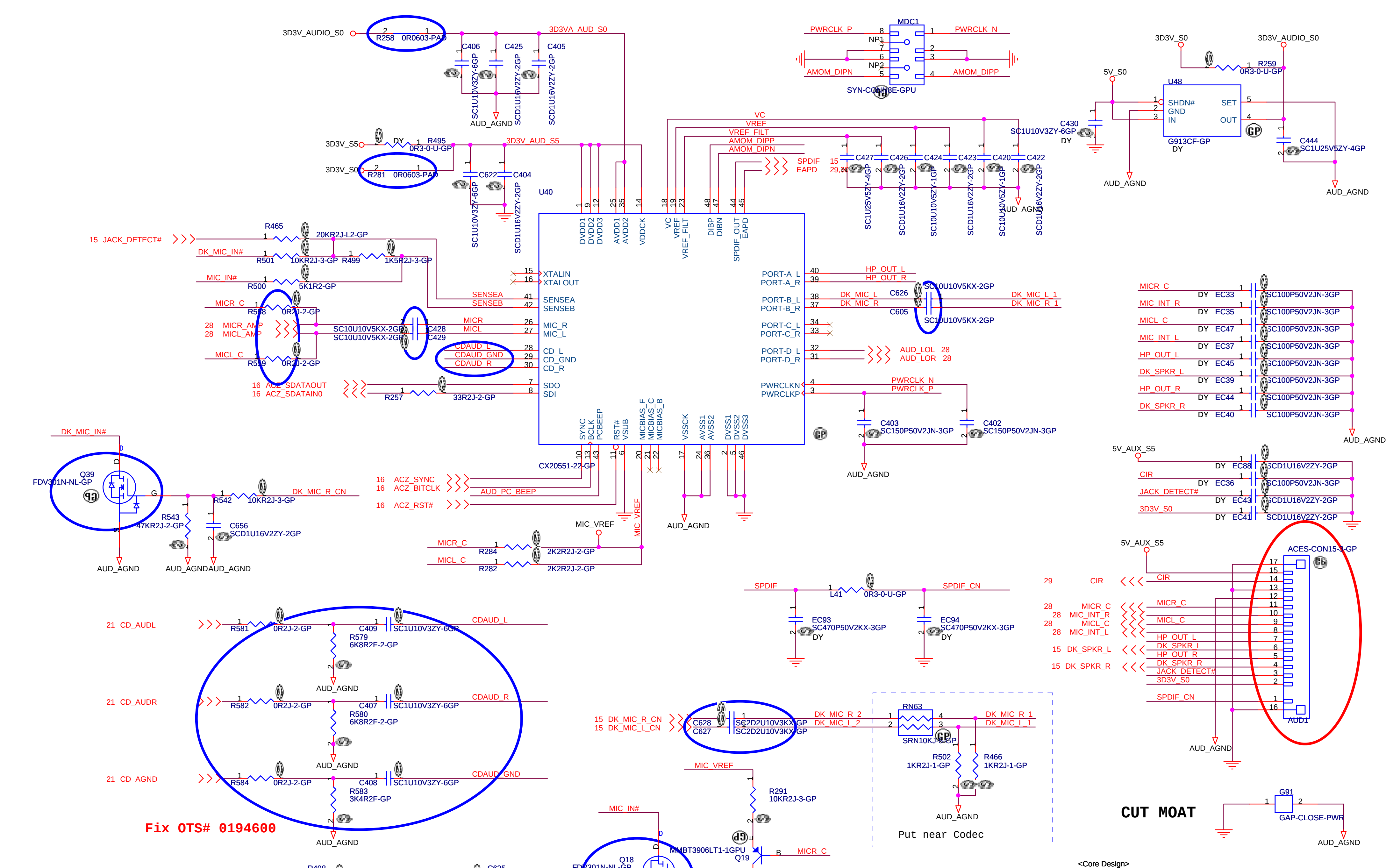
10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

NEWCARD Connector





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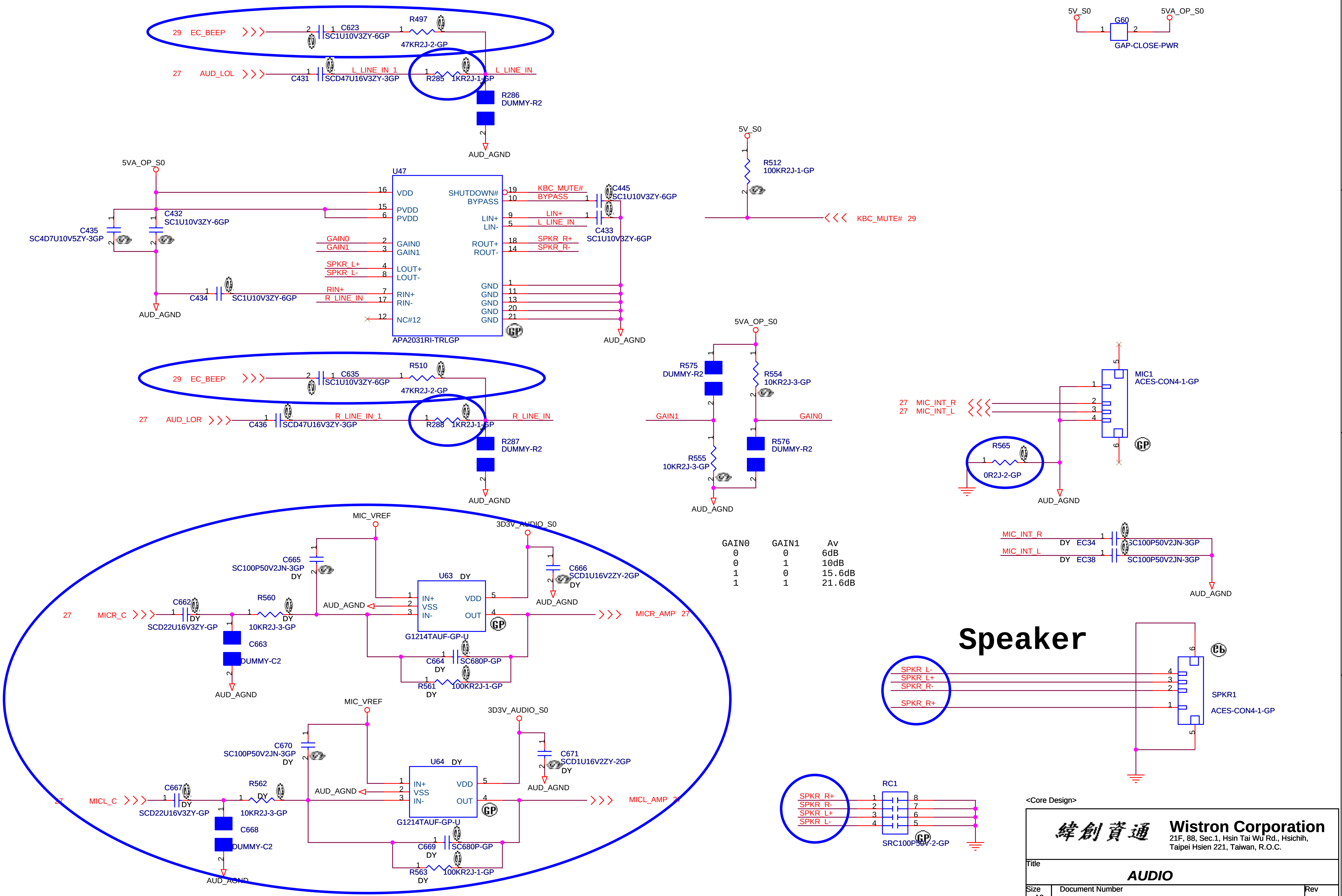
Title	AUDIO CODEC AD1981B	
Size A3	Document Number KAI	Rev SE
Date: Thursday, June 22, 2006	Sheet 27 of 44	



GAIN0	GAIN1	Av
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

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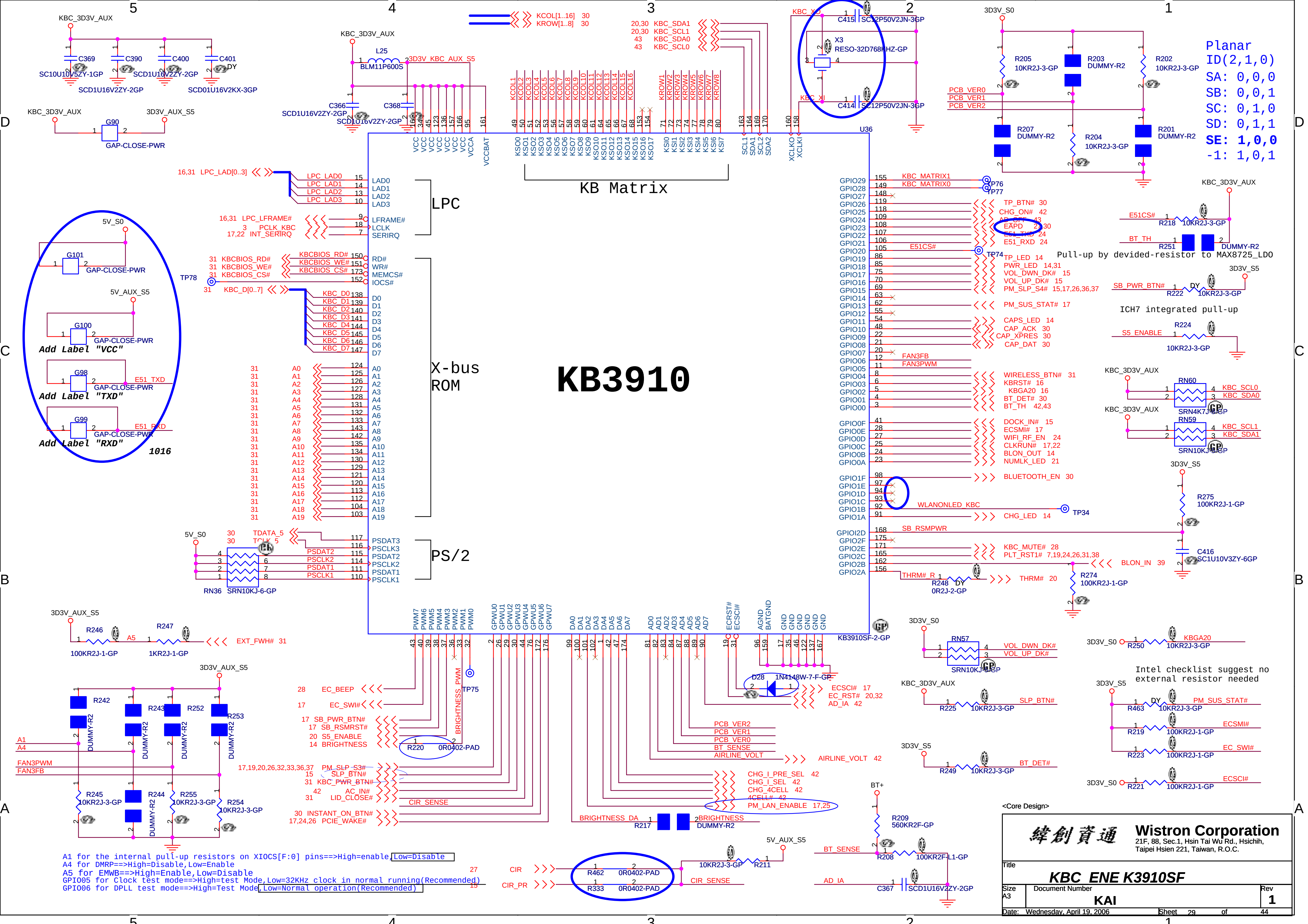
Title: **AUDIO**

Size: A3 | Document Number: KAI | Rev: SE

Date: Tuesday, May 23, 2006 | Sheet 28 of 44


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U36
KB3910SF-2-GP
Planar ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Intel checklist suggest no external resistor needed
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
1016
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC_ENE K3910SF
Size A3
Document Number
KAI
Rev 1
Date: Wednesday, April 19, 2006
Sheet 29 of 44

CAMERA

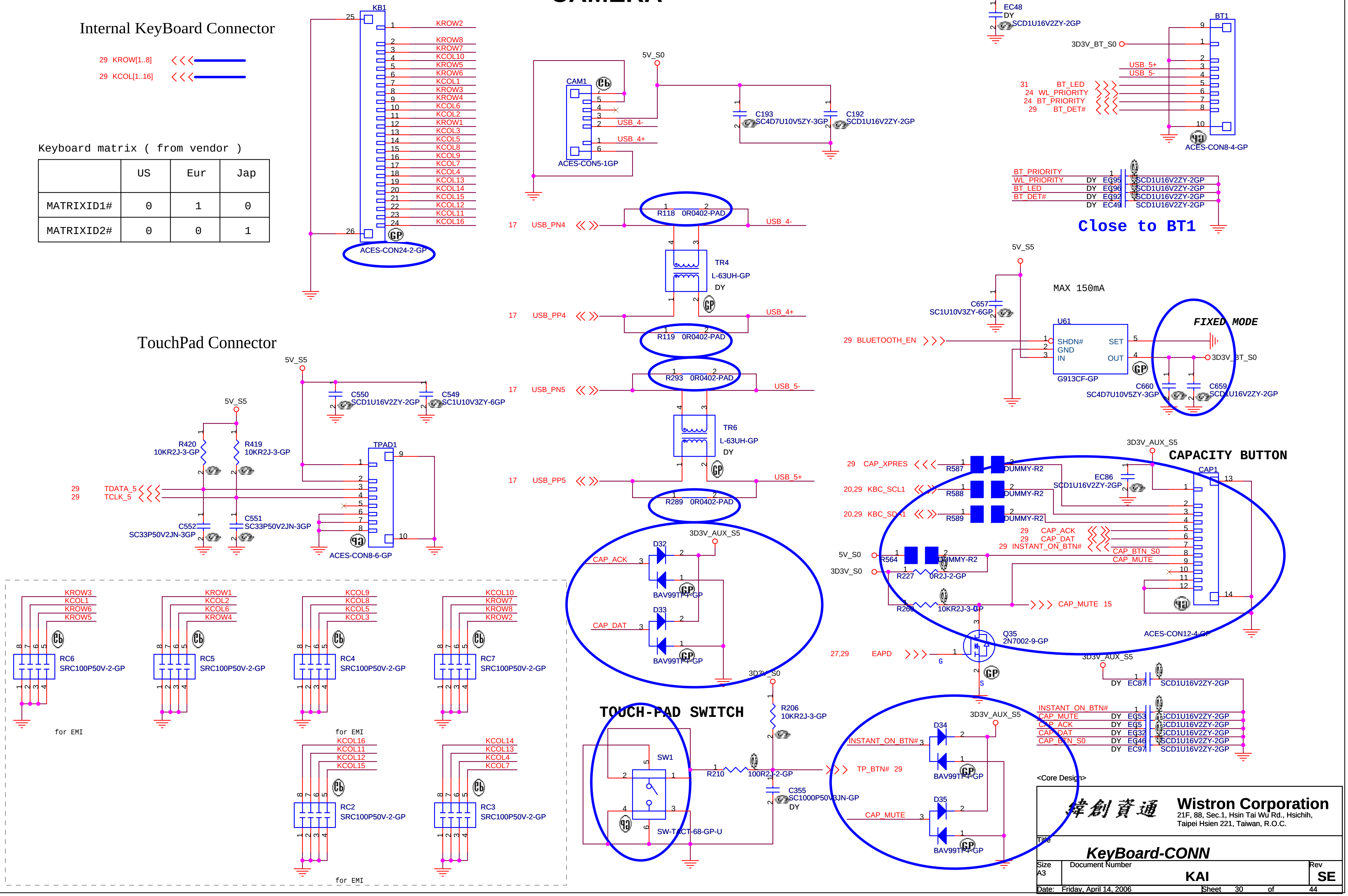
Blue thumb

Internal KeyBoard Connector

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

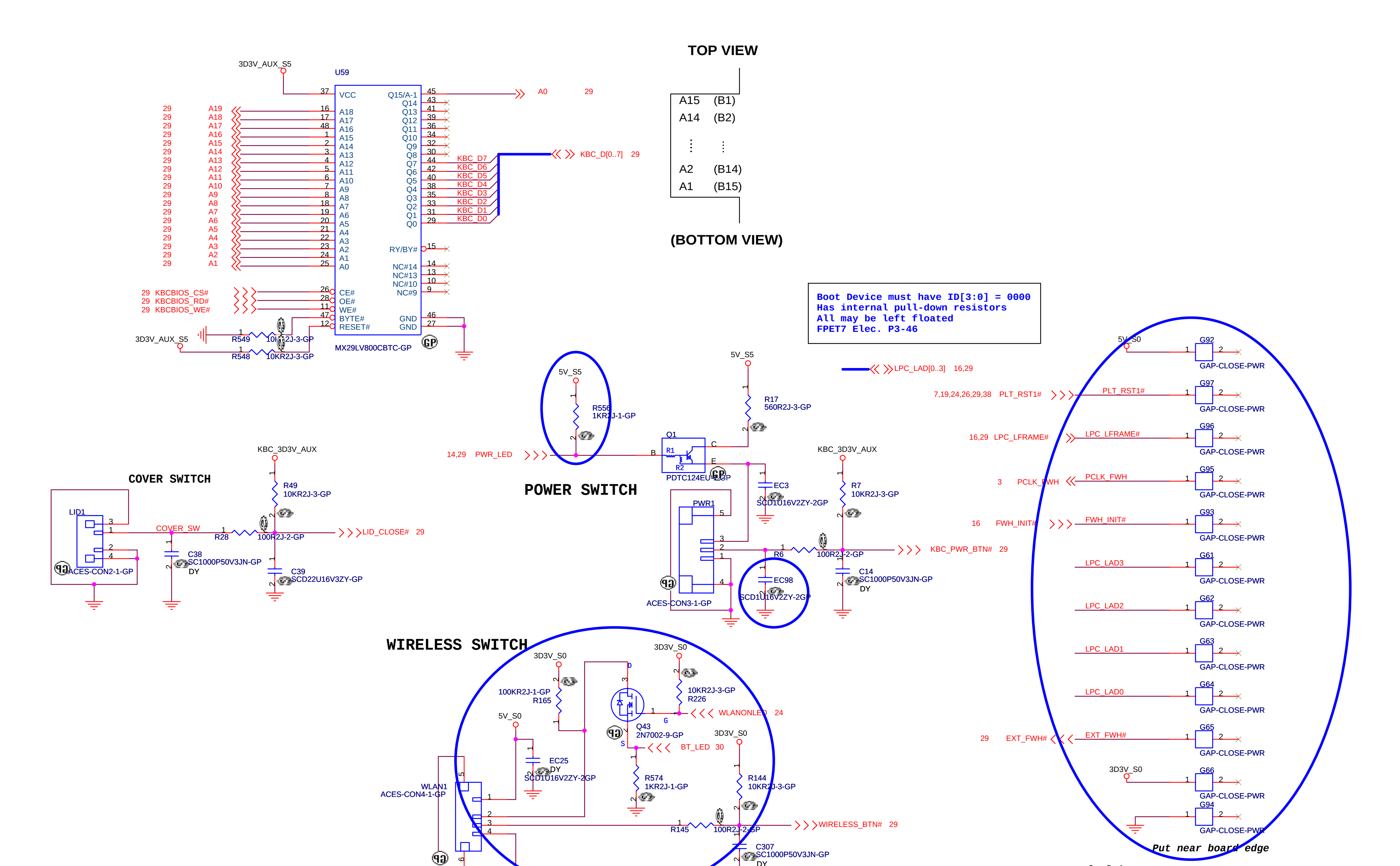
TouchPad Connector



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

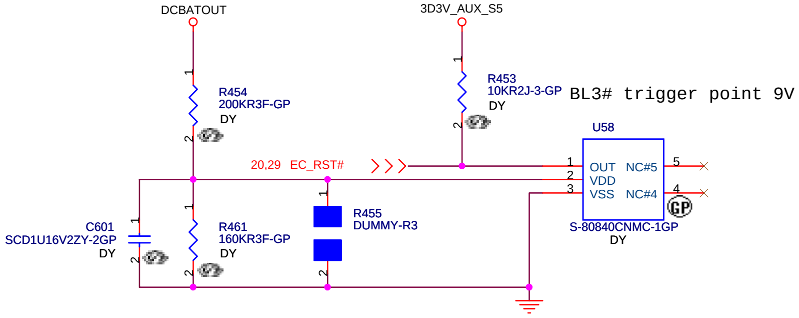
Title	KeyBoard-CONN	
Size A3	Document Number KAI	Rev SE
Date: Friday, April 14, 2006	Sheet 30 of 44	



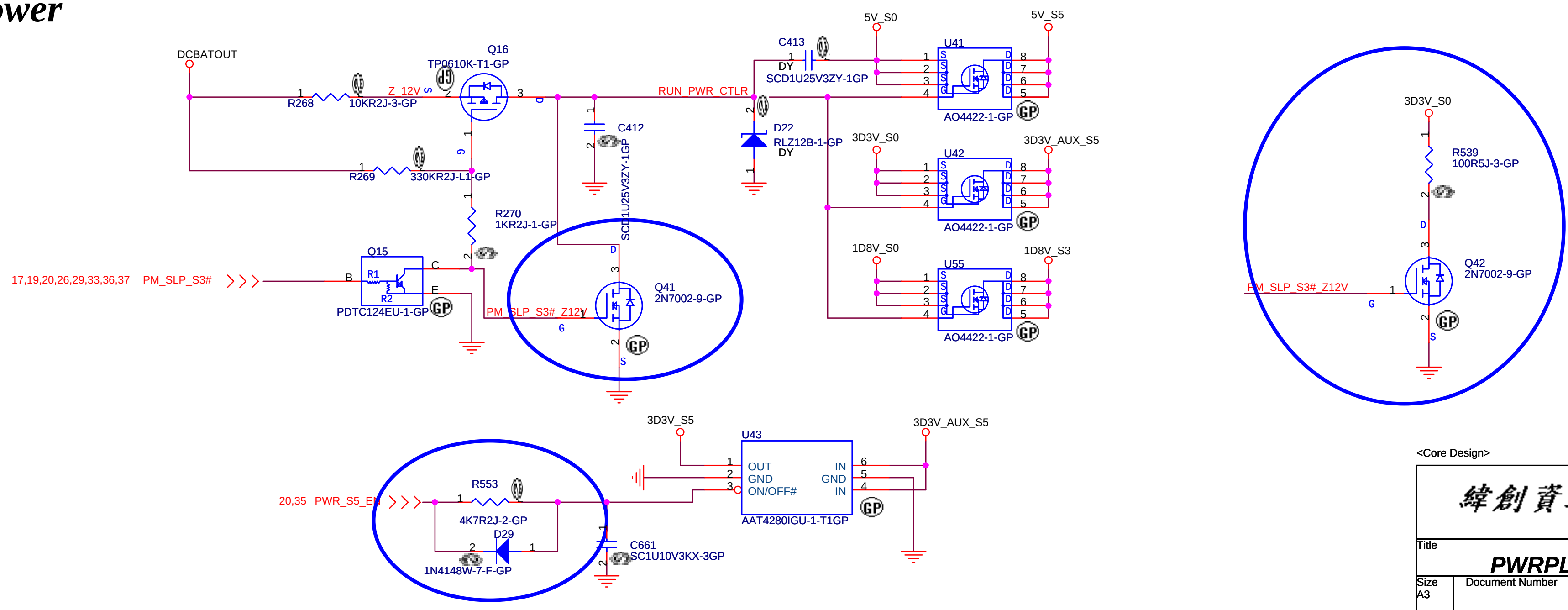
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	FWH and Debug	
Size A3	Document Number KAI	Rev SE
Date: Friday, April 14, 2006	Sheet 31 of 44	



Run Power

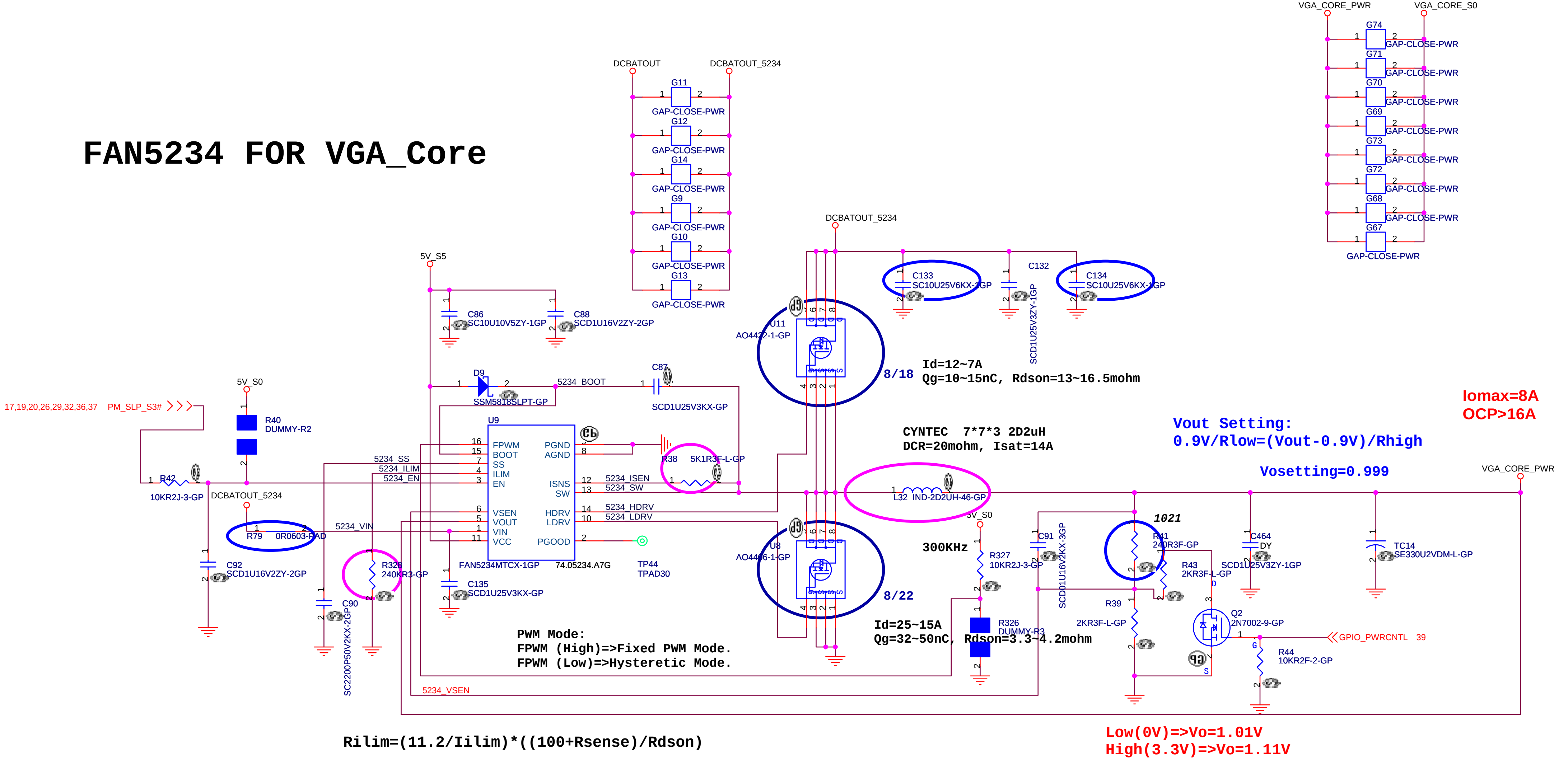


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	PWRPLANE&RESETLOGIC	
Size A3	Document Number KAI	Rev SE
Date: Wednesday, May 17, 2006	Sheet 32 of 44	

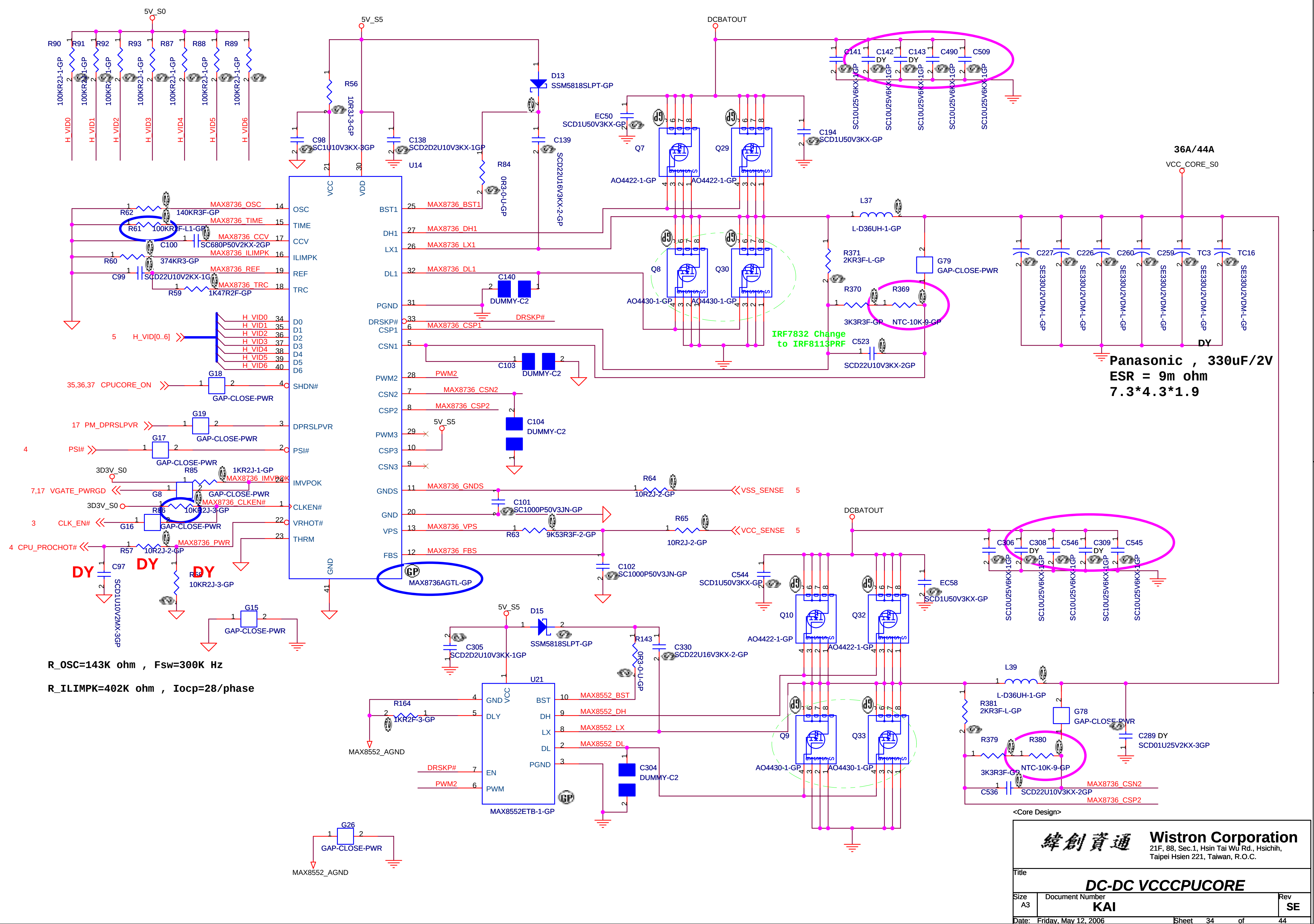
FAN5234 FOR VGA_Core

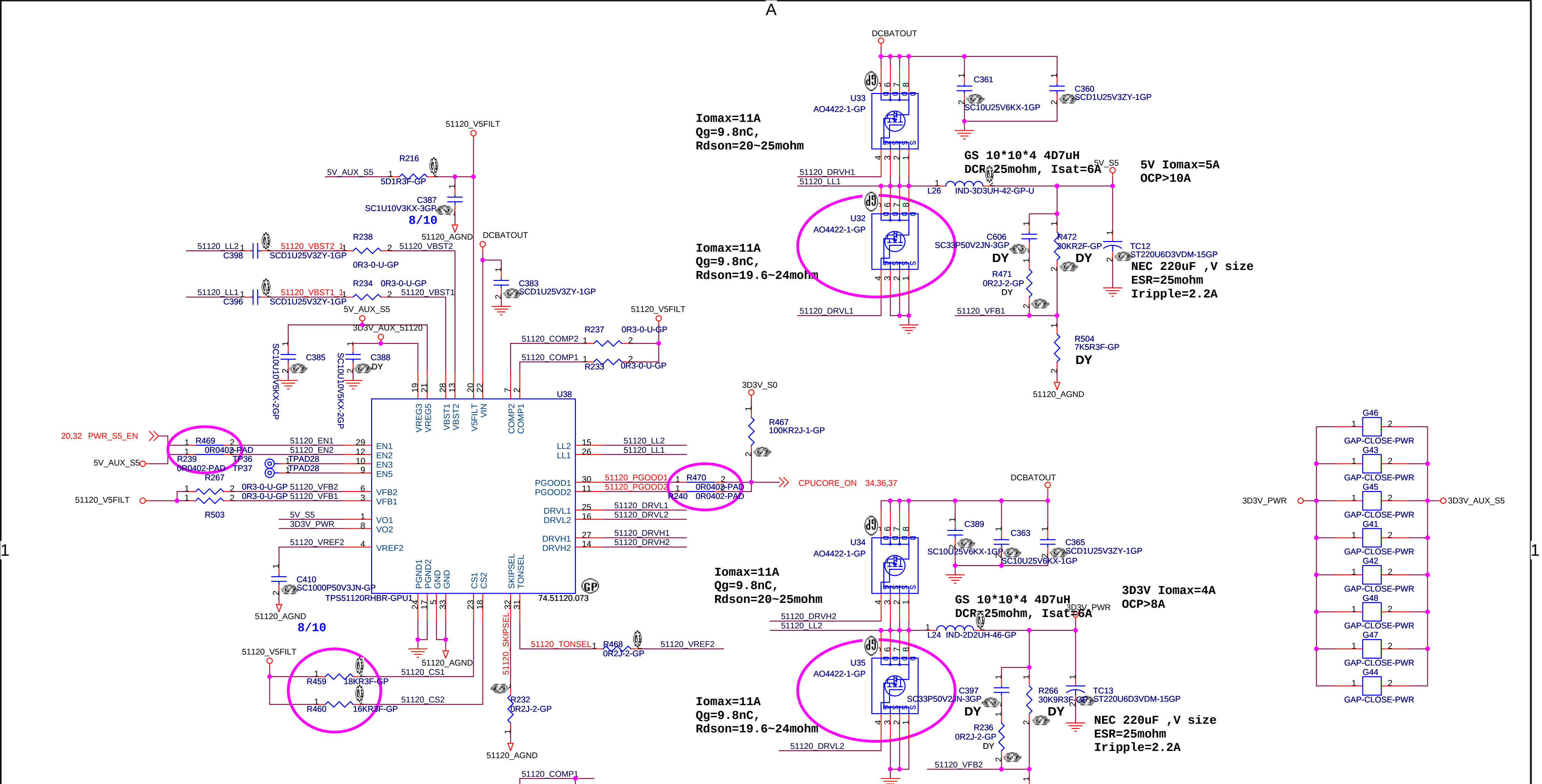


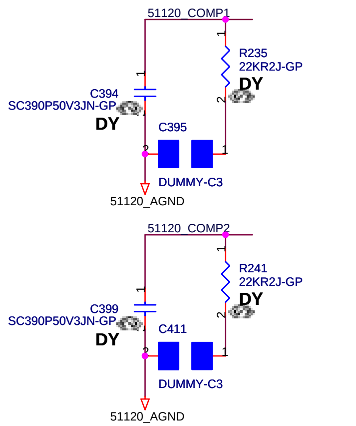
<Core Design>

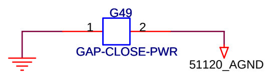
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VGA CORE 1V	
Size A3	Document Number TACOMA	Rev SE
Date: Friday, April 14, 2006	Sheet 33 of 44	


5V_S0
R90
R91
R92
R93
R87
R88
R89
100KR2J-1-GP
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
5V_S5
R56
10R3J-3-GP
C98
SC1U10V3KX-3GP
C138
SCD2D2U10V3KX-1GP
U14
D13
SSM5818SLPT-GP
C139
SCD22U16V3KX-2-GP
R84
0R3-0-U-GP
DCBATOUT
EC50
SCD1U50V3KX-GP
Q7
Q29
AO4422-1-GP
C194
SCD1U50V3KX-GP
C141
C142
C143
C490
C509
DY
SC10U25V6KX-1GP
36A/44A
VCC_CORE_S0
MAX8736_OSC
MAX8736_TIME
MAX8736_CCV
MAX8736_ILIMPK
MAX8736_REF
MAX8736_TRC
R62
140KR3F-GP
R61
100KR2F-L1-GP
C100
SC680P50V2KX-2GP
R60
374KR3-GP
C99
SCD22U10V2KX-1GP
R59
1K47R2F-GP
OSC
TIME
CCV
ILIMPK
REF
TRC
VCC
VDD
BST1
DH1
LX1
DL1
PGND
DRSKP#
CSP1
CSN1
PWM2
CSN2
CSP2
PWM3
CSP3
CSN3
GNDS
GND
VPS
FBS
MAX8736_BST1
MAX8736_DH1
MAX8736_LX1
MAX8736_DL1
C140
DUMMY-C2
DRSKP#
MAX8736_CSP1
C103
MAX8736_CSN2
MAX8736_CSP2
C104
Q8
Q30
AO4430-1-GP
IRF7832 Change
to IRF8113PRF
L37
L-D36UH-1-GP
R371
2KR3F-L-GP
G79
GAP-CLOSE-PWR
R370
R369
3K3R3F-GP
NTC-10K-9-GP
C523
SCD22U10V3KX-2GP
C227
C226
C260
C259
TC3
TC16
SE330U2VDM-L-GP
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
D0
D1
D2
D3
D4
D5
D6
H_VID[0..6]
35,36,37 CPUCORE_ON
G18
SHDN#
17 PM_DPRSLPVR
G19
DPRSLPVR
PSI#
G17
PSI#
3D3V_S0
R85
1KR2J-1-GP
MAX8736_IMVPOK
IMVPOK
7,17 VGATE_PWRGD
G8
3D3V_S0
R86
10KR2J-3-GP
MAX8736_CLKEN#
CLKEN#
3 CLK_EN#
G16
VRHOT#
THRM
4 CPU_PROCHOT#
R57
10R2J-2-GP
MAX8736_PWR
C97
SCD1U10V2MX-3GP
R58
10KR2J-3-GP
G15
MAX8736AGTL-GP
MAX8736_GNDS
C101
SC1000P50V3JN-GP
MAX8736_VPS
R63
9K53R3F-2-GP
MAX8736_FBS
C102
SC1000P50V3JN-GP
R64
10R2J-2-GP
VSS_SENSE 5
R65
10R2J-2-GP
VCC_SENSE 5
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
5V_S5
D15
SSM5818SLPT-GP
C305
SCD2D2U10V3KX-1GP
R143
0R3-0-U-GP
C330
SCD22U16V3KX-2-GP
U21
GND
DLY
BST
DH
LX
DL
PGND
EN
PWM
MAX8552_BST
MAX8552_DH
MAX8552_LX
MAX8552_DL
R164
1KR2F-3-GP
MAX8552_AGND
C304
DUMMY-C2
MAX8552ETB-1-GP
G26
GAP-CLOSE-PWR
MAX8552_AGND
C544
SCD1U50V3KX-GP
Q10
Q32
EC58
SCD1U50V3KX-GP
C306
C308
C546
C309
C545
SC10U25V6KX-1GP
Q9
Q33
L39
L-D36UH-1-GP
R381
2KR3F-L-GP
G78
GAP-CLOSE-PWR
C289 DY
SCD01U25V2KX-3GP
R379
R380
3K3R3F-GP
NTC-10K-9-GP
C536
SCD22U10V3KX-2GP
MAX8736_CSN2
MAX8736_CSP2
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC-DC VCCCPUCORE
Size A3
Document Number KAI
Rev SE
Date: Friday, May 12, 2006
Sheet 34 of 44







Vout=1V*(R1+R2)/R2

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

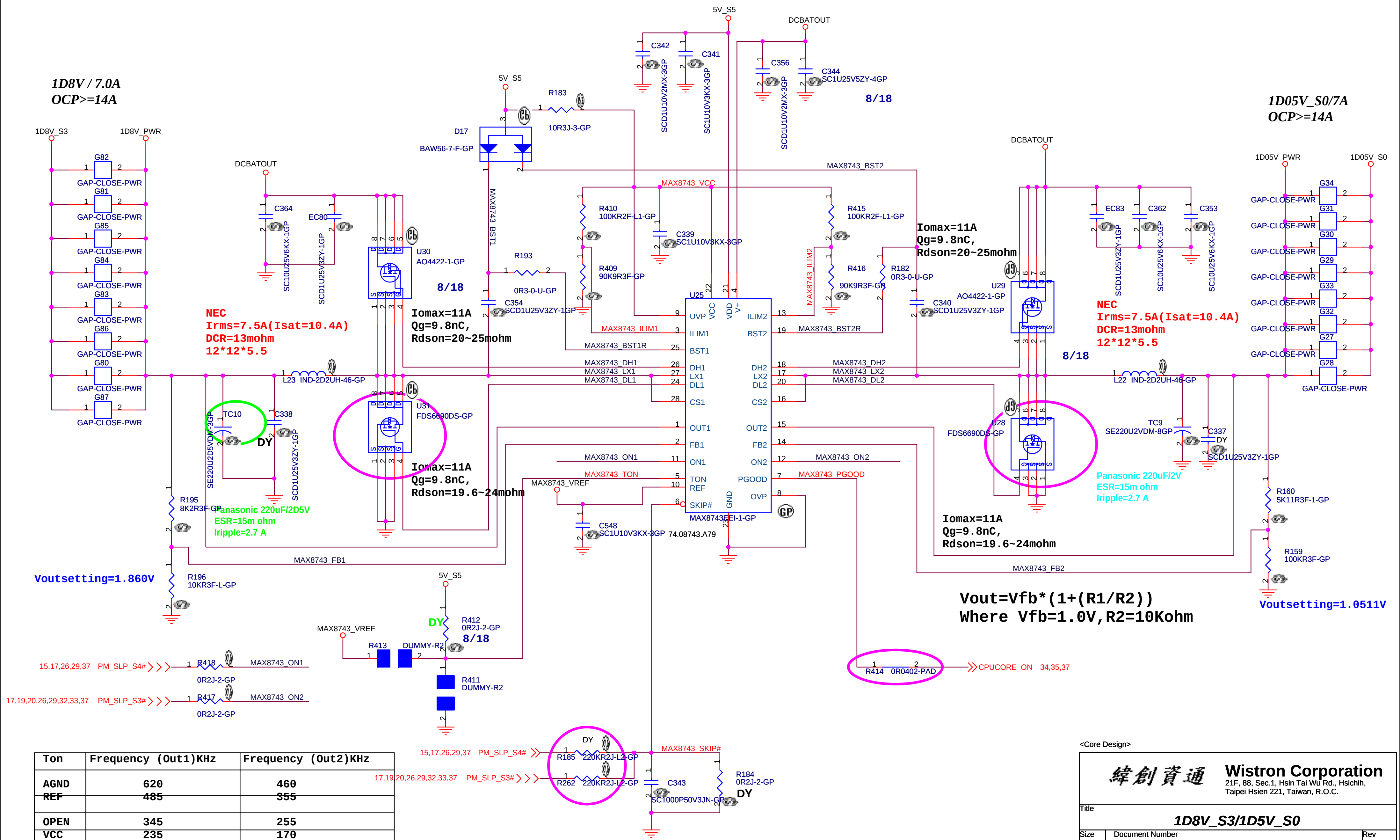
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
5V_S5/3D3V_S5			
Size: A3	Document Number: KAI		Rev: SE
Date: Thursday, April 13, 2006	Sheet 35	of 44	

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

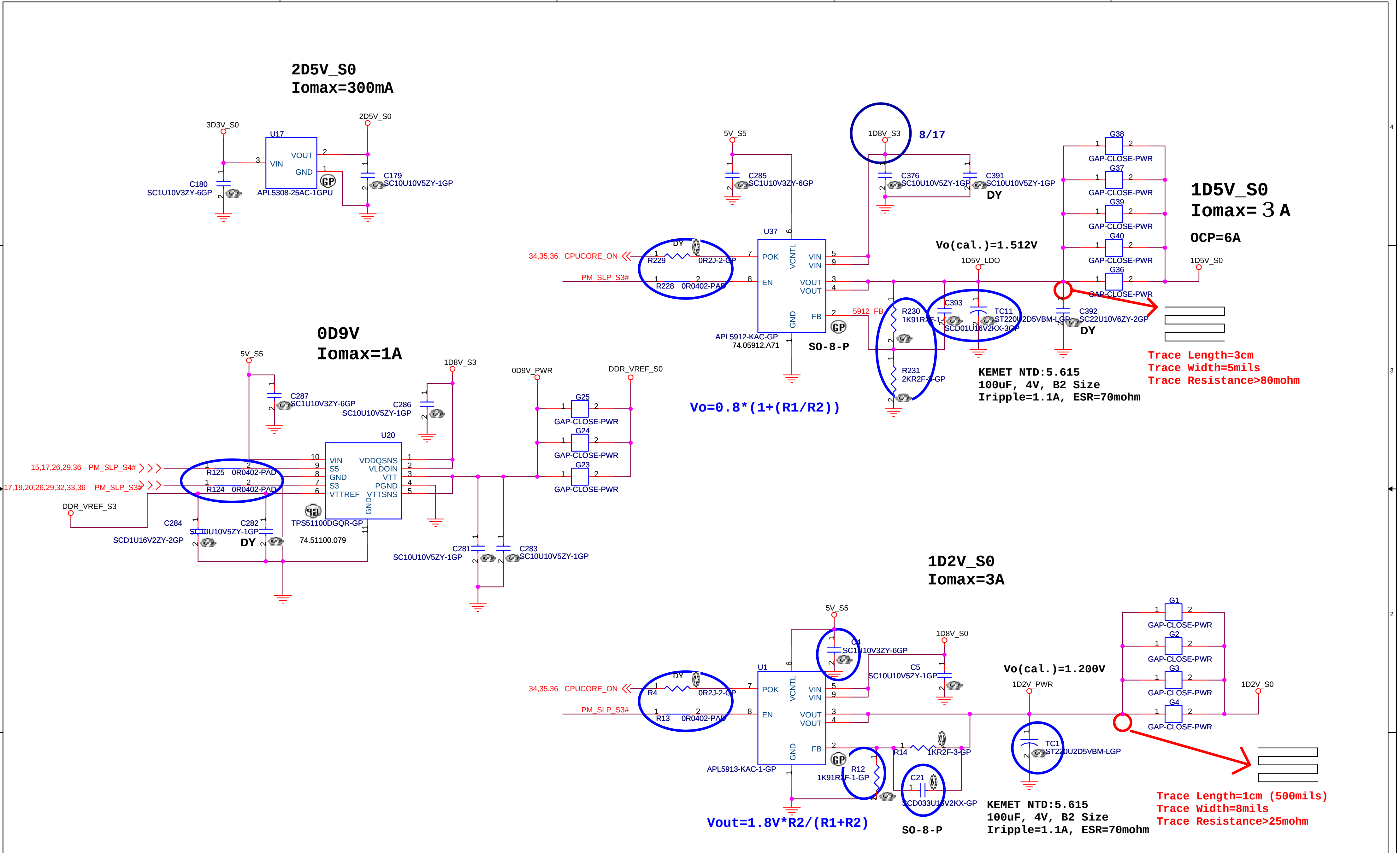


Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

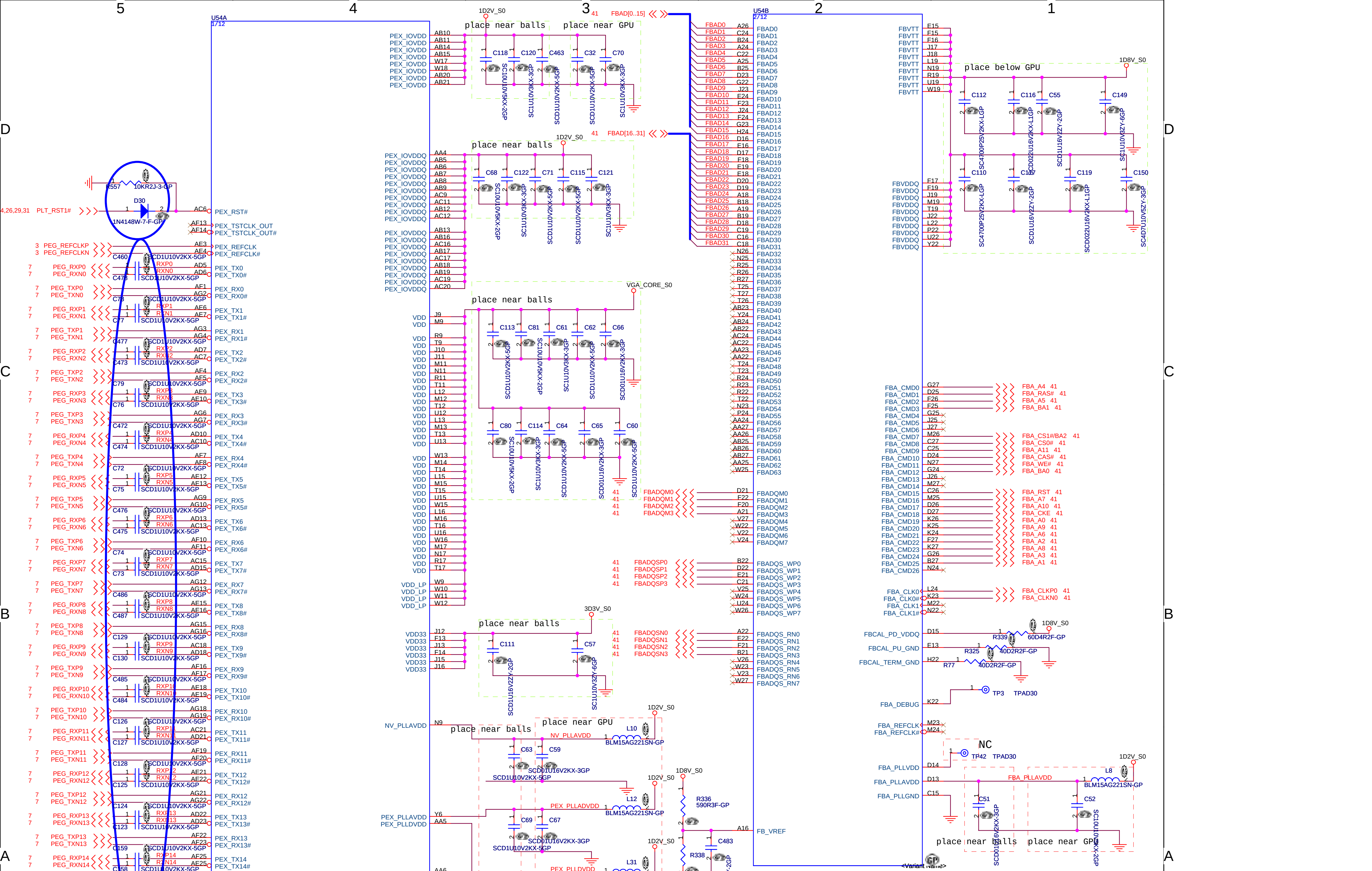
Title	1D8V_S3/1D5V_S0	
Size A3	Document Number KAI	Rev SE
Date: Monday, March 27, 2006	Sheet 36 of 44	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO		
Size: A3	Document Number: KAI	Rev: SE
Date: Monday, March 27, 2006	Sheet 37 of 44	

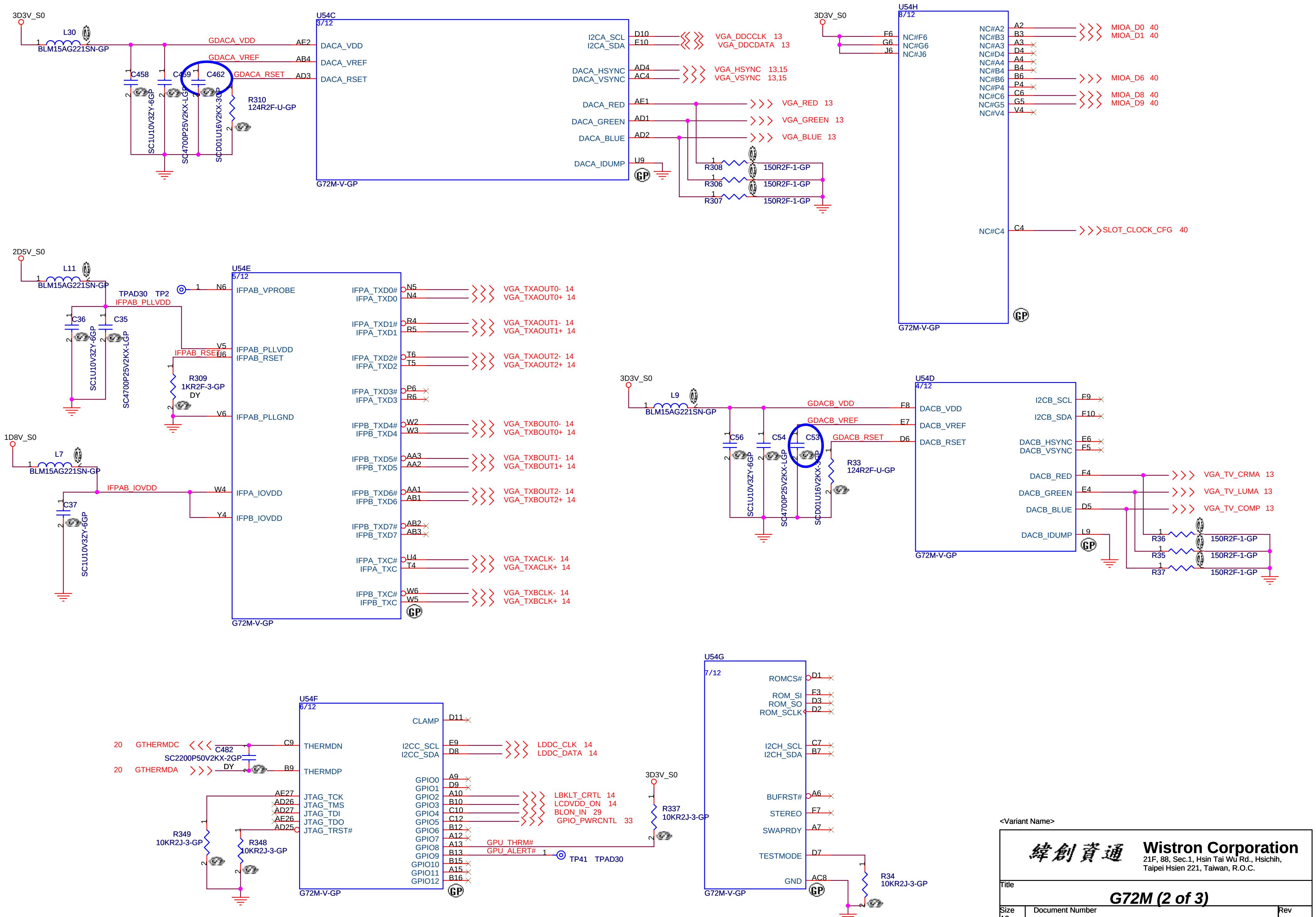


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M (1 of 3)

Size: Custom | Document Number: KAI | Rev: SD

Date: Wednesday, April 19, 2006 | Sheet 38 of 44



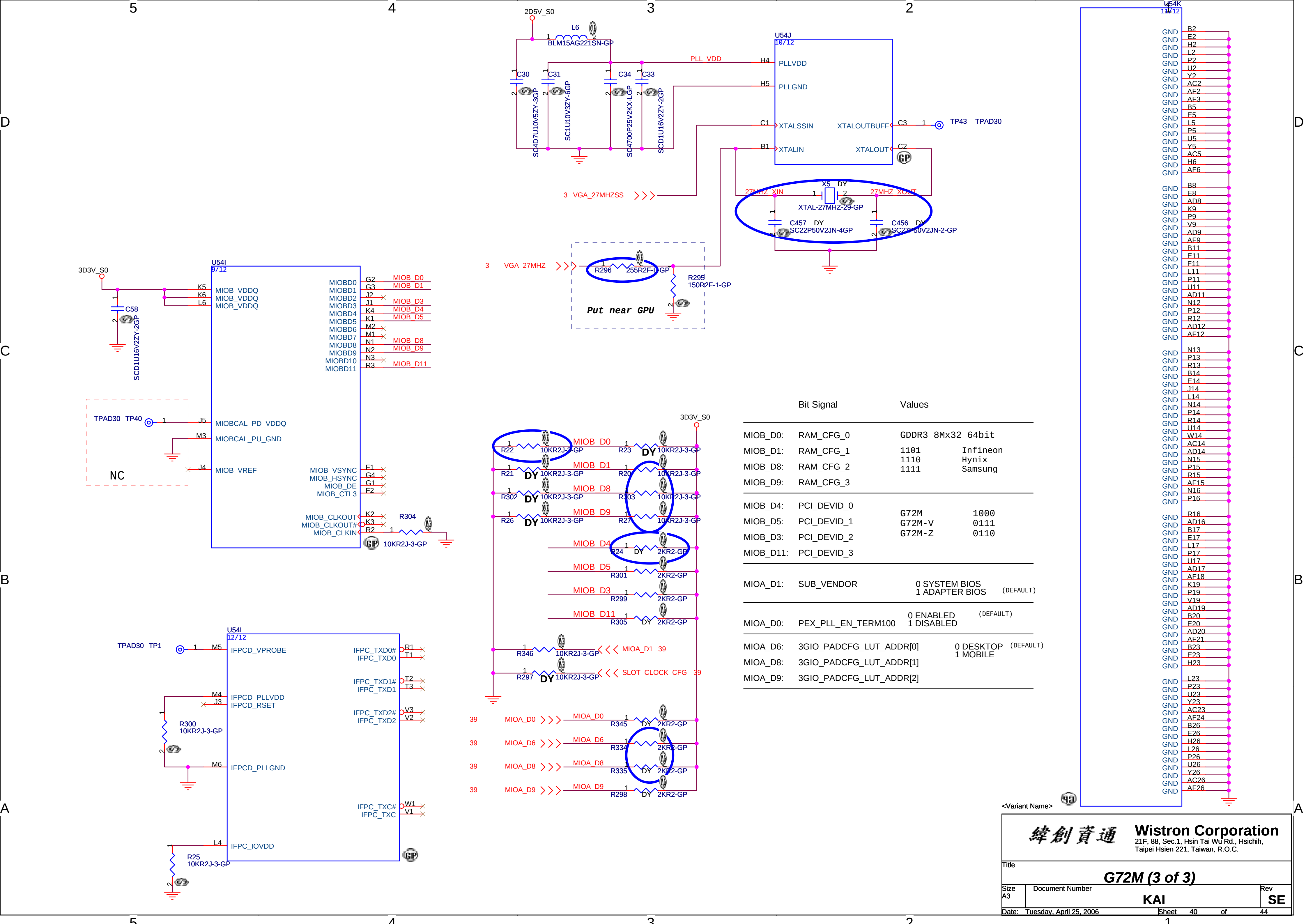
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
G72M (2 of 3)

Size	Document Number	Rev
A3	KAI	SE

Date: Wednesday, April 19, 2006 Sheet 39 of 44



Bit	Signal	Values	
MIOB_D0:	RAM_CFG_0	GDDR3 8Mx32 64bit	
MIOB_D1:	RAM_CFG_1	1101 1110 1111	Infineon Hynix Samsung
MIOB_D8:	RAM_CFG_2		
MIOB_D9:	RAM_CFG_3		
MIOB_D4:	PCI_DEVID_0	G72M G72M-V G72M-Z	1000 0111 0110
MIOB_D5:	PCI_DEVID_1		
MIOB_D3:	PCI_DEVID_2		
MIOB_D11:	PCI_DEVID_3		
MIOA_D1:	SUB_VENDOR	0 SYSTEM BIOS (DEFAULT) 1 ADAPTER BIOS	
MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED (DEFAULT) 1 DISABLED	
MIOA_D6:	3GIO_PADCFG_LUT_ADDR[0]	0 DESKTOP (DEFAULT) 1 MOBILE	
MIOA_D8:	3GIO_PADCFG_LUT_ADDR[1]		
MIOA_D9:	3GIO_PADCFG_LUT_ADDR[2]		

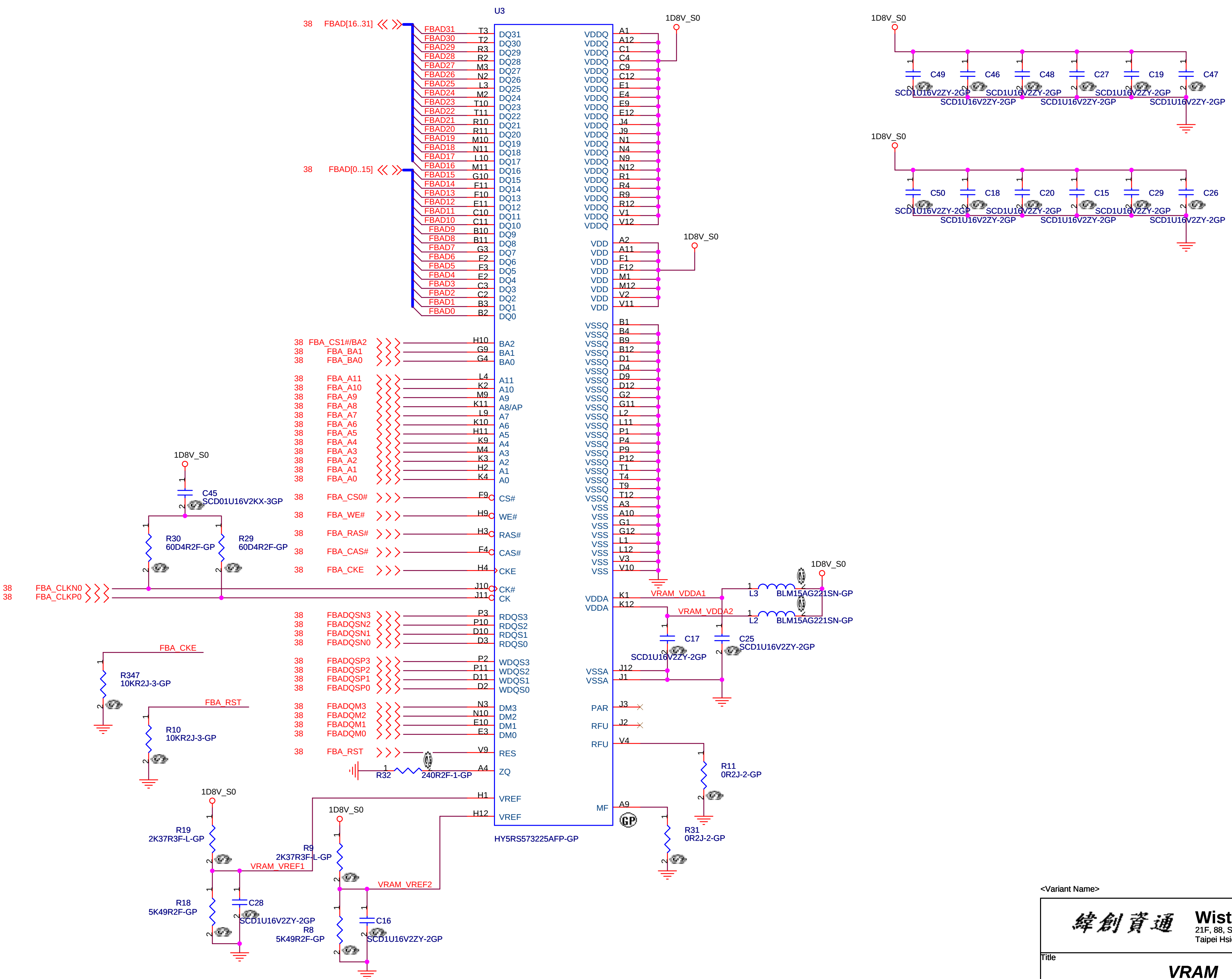
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **G72M (3 of 3)**

Size: A3 | Document Number: KAI | Rev: SE

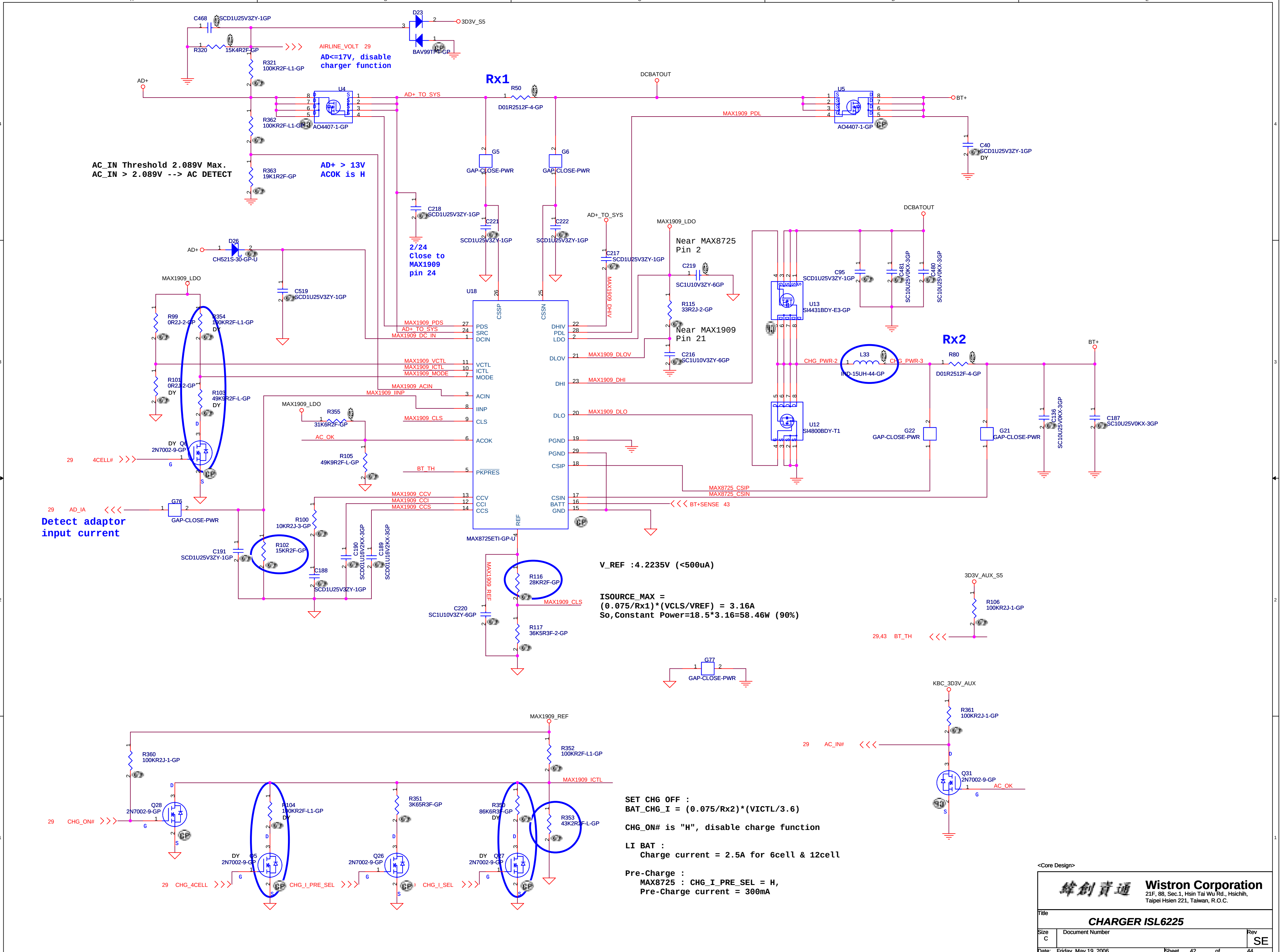
Date: Tuesday, April 25, 2006 | Sheet 40 of 44

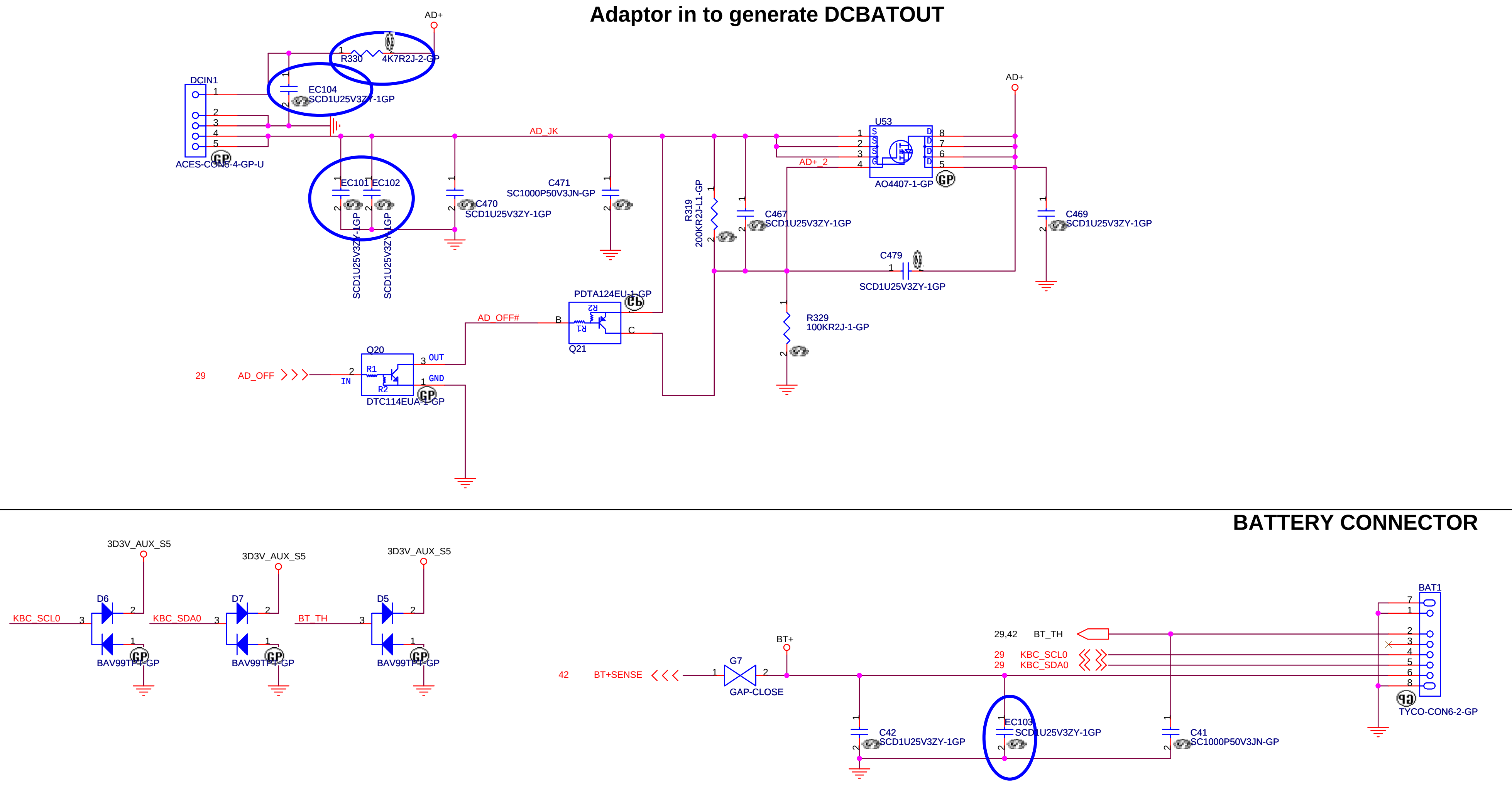


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**VRAM**	
Size A3	Document Number **KAI**	Rev **SD**
Date: Wednesday, April 19, 2006	Sheet 41 of 44	

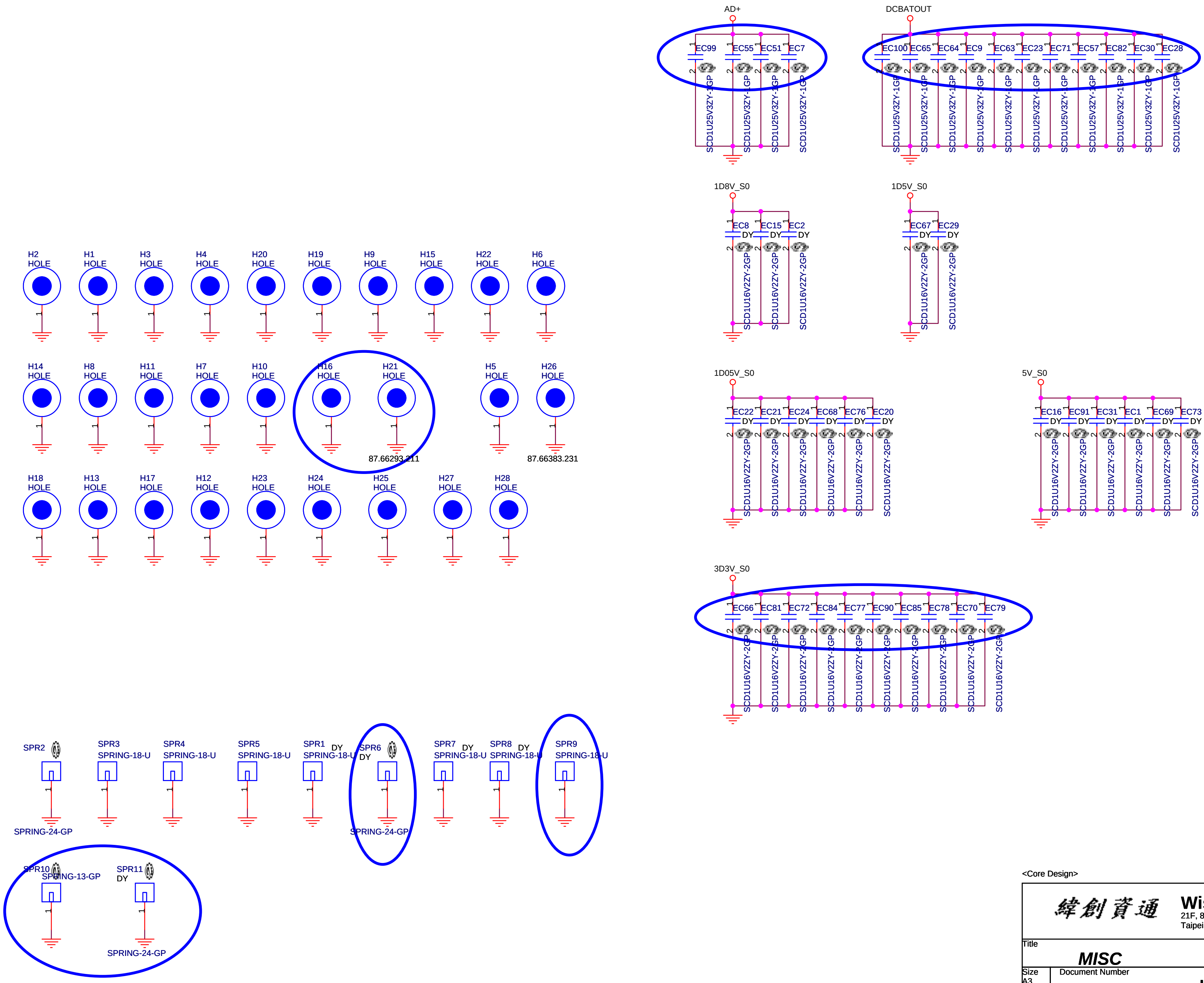

AD<=17V, disable charger function
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
Rx1
Rx2
2/24
Close to
MAX1909
pin 24
Near MAX8725
Pin 2
Near MAX1909
Pin 21
Detect adaptor
input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
CHG_ON# is "H", disable charge function
LI BAT :
Charge current = 2.5A for 6cell & 12cell
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
U18
MAX8725ETI-GP-U
U4
AO4407-1-GP
U5
AO4407-1-GP
U13
SI4431BDY-E3-GP
U12
SI4800BDY-T1
L33
IND-15UH-44-GP
R50
D01R2512F-4-GP
R80
D01R2512F-4-GP
DCBATOUT
BT+
AD+
3D3V_S5
MAX1909_LDO
MAX1909_REF
3D3V_AUX_S5
KBC_3D3V_AUX
AIRLINE_VOLT 29
AD_IA
BT+SENSE 43
BT_TH
AC_IN#
AC_OK
CHG_ON#
CHG_4CELL
CHG_I_PRE_SEL
CHG_I_SEL
4CELL#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER ISL6225
Size C
Document Number
Rev SE
Date: Friday, May 19, 2006
Sheet 42 of 44



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**		
Size: A3	Document Number	Rev: SE
Date: Monday, March 27, 2006	Sheet 43 of 44	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *MISC*		
Size: A3	Document Number: KAI	Rev: SE
Date: Thursday, April 13, 2006	Sheet 44 of 44	