### RESISTOR

<table>
<thead>
<tr>
<th>Symbol name</th>
<th>Value</th>
<th>Tolerance</th>
<th>Rating</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>10KR3</td>
<td>10K Ohm</td>
<td>If no letter, it means J: 5%</td>
<td>1/16W, 75V</td>
<td>0603</td>
</tr>
<tr>
<td>333KR5</td>
<td>33.3 Ohm</td>
<td>If no letter, it means J: 5%</td>
<td>1/10W, 100V</td>
<td>0805</td>
</tr>
<tr>
<td>1KR3</td>
<td>1K Ohm</td>
<td>F: 1%</td>
<td>1/16W, 75V</td>
<td>0603</td>
</tr>
</tbody>
</table>

*The naming rule is value + R + size + tolerance*

*For the value, it can be read by the number before R. (R means resistor)*

*For the tolerance, it can be read from the last letter.*

*For the rating, we don't show on the symbol name.*

*For the size, R2=>0402, R3=>0603, R5=>0805....*

### CAPACITOR

<table>
<thead>
<tr>
<th>Symbol name</th>
<th>Value</th>
<th>Tolerance</th>
<th>Rating</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCD1U010V2M1X-1</td>
<td>0.1uF</td>
<td>M/X5R</td>
<td>10V</td>
<td>0402</td>
</tr>
<tr>
<td>SCD16U035V9M-1X-1</td>
<td>10uF</td>
<td>M/X5R</td>
<td>6.3V</td>
<td>0605</td>
</tr>
<tr>
<td>SCD2U035V62-1</td>
<td>2.2uF</td>
<td>Z/Y5V</td>
<td>16V</td>
<td>0605</td>
</tr>
</tbody>
</table>

*The naming rule is value + rating + size + tolerance + material*

*SCD1U010V2M1X-1*

*SCD16U035V9M-1X-1*

*SCD2U035V62-1*

*Symbol name: SMT Ceramic, TC=> POS cap or SP cap*

*1uF => 0.1uF*

*10V => the voltage rating is 10V*

*2=>0402, 3=>0603, 5=>0805*

*M: tolerance M, K, Z*

*X: X7R/X5R, Y: Y5V*

*-1 => symbol version, nonsense to EE characteristic*

### PLANNER ID[3..0]

<table>
<thead>
<tr>
<th>PCI GP</th>
<th>Planar PCI Version</th>
<th>Planar ID Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>3784</td>
<td>PCH GPOn</td>
<td>Pellan_IDn</td>
</tr>
<tr>
<td>0000</td>
<td>SDV</td>
<td>0</td>
</tr>
<tr>
<td>0001</td>
<td>SDV</td>
<td>1</td>
</tr>
<tr>
<td>0010</td>
<td>FVT</td>
<td>0</td>
</tr>
<tr>
<td>0011</td>
<td>BISB</td>
<td>1</td>
</tr>
<tr>
<td>0110</td>
<td>SVT</td>
<td>0</td>
</tr>
<tr>
<td>0111</td>
<td>SVT</td>
<td>1</td>
</tr>
<tr>
<td>1000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1010</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1101</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1111</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### PCI TABLE

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>IDSEL</th>
<th>IRQ (Default)</th>
<th>REQ# / GNT#</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINPCI SLOT</td>
<td>AD16</td>
<td>F, G</td>
<td>REQ# 3 / GNT#</td>
</tr>
<tr>
<td>CARDBUS R5CB11</td>
<td>AD16</td>
<td>SERIRQ</td>
<td>REQ#0 / GNT#</td>
</tr>
<tr>
<td>USB UHCI</td>
<td>AD29</td>
<td>A, C, D</td>
<td></td>
</tr>
<tr>
<td>USB 2.0 EHCI</td>
<td>AD29</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>DMI to PCI/ AC97 Modem/ AC97 Audio</td>
<td>AD30</td>
<td>B</td>
<td></td>
</tr>
<tr>
<td>LPC Bridge IDE</td>
<td>AD31</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>LPC Bridge SATA</td>
<td>AD31</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PCIe Express</td>
<td>AD29</td>
<td>A, B, C, D</td>
<td></td>
</tr>
</tbody>
</table>

### EC HISTORY

<table>
<thead>
<tr>
<th>Stage</th>
<th>Date</th>
<th>EC No.</th>
<th>Page</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDV</td>
<td>-</td>
<td>-</td>
<td>0603</td>
<td></td>
</tr>
</tbody>
</table>

*Wistron Corporation 21F, 88, Sec.1, Hsin Ti W u Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.*

*Planar PCB Version*
From Cougar Point

To Cougar Point

To Cougar Point

From Cougar Point

These PEG interface is left as NC, if external GFX is not mounted.

if external GFX is not mounted..
Need to refer Intel Design Guide to place CPU and route wire.

SNB_IVB# is used for control of TacomaPass CLE.

SKTOCC# pin is tied down by CPU, when CPU is inserted at socket.

To power shutdown circuits
Open Drain Output
0.9V~3.6V operation device

Catastrophic error output

This test point is used at PCB house process.

Place near CPU

Place near CPU

This change is to S3 Wake up issue based on Intel White paper

Need to find Schmitt with Open drain output

Place near DIMM connector
When PEG Defer training function is used, CFG7 should have pull down. When PCIe Port Bifurcation function is used, CFG5 & 6 should have pull down.

Low/Low : x8 , x4 and x4
Low/High : Reserved
High/Low : x8 and x8
High/High : x16

eDP Function is used, CFG4 port should be tie Down. If not, this port can be left as floating.

When PEG Lane reversible function is used, CFG2 should have pull down.

Should be add pulldown 1K based on configuration specification.
This jumper is placed to monitor current.

Take care PullUp/PullDown resistor placement.[Should be minimized stub.]
When Igfx is disabled, these lines can be left floating.
In production, all of parts should be not mounted except of pulldown 51 ohm on TCK.

**DEBUG Interface for PCH.**

PCH XDP SFF 26pin IF
Pin 1 OBSFN_A0 (Open, I/O)
Pin 2 OBSFN_A1 (Open, I/O)
Pin 3 GND
Pin 4 OBSIDATA_A0 (Open, I/O)
Pin 5 OBSIDATA_A1 (Open, I/O)
Pin 6 GND
Pin 7 OBSIDATA_A2 (Open, I/O)
Pin 8 OBSIDATA_A3 (Open, I/O)
Pin 9 GND
Pin 10 HOOK0 (PWRGD, In)
Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
Pin 12 HOOK2 (CFG0, Out)
Pin 13 HOOK3 (DBR#, Out)
Pin 14 HOOK4 (BCLK, In)
Pin 15 HOOK5 (BCLK#, In)
Pin 16 VCCOBS_AB (VCCP Voltage of CPU, Out)
Pin 17 HOOK6 (RESETP, Out)
Pin 18 HOOK7 (BP_PWRGD_RST#, Out)
Pin 19 GND
Pin 20 TDO, In
Pin 21 TRST#, Out
Pin 22 TDI, Out
Pin 23 TMS, Out
Pin 24 TCK (Open)
Pin 25 GND
Pin 26 TCK0, Out

---

**XDP CONNECTOR**

Kendo-3 WS

**BOM**

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
This connector should be placed on far side from CPU.
TABLE KENDO VIDEO MEMORY

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>HY57V128800</th>
<th>HY57V256800</th>
</tr>
</thead>
<tbody>
<tr>
<td>HYNIX</td>
<td>128Mx16</td>
<td>256Mx16</td>
</tr>
<tr>
<td>SAMSUNG</td>
<td>128Mx16</td>
<td>256Mx16</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RO M_SIP7 H6238</th>
<th>34.8Kohm</th>
<th>45.3Kohm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>64.4525.6DL</td>
<td>64.4532.6DL</td>
</tr>
</tbody>
</table>
FBCLK Termination
If strap is sampled high.

Integrated Deep Sleep 54:55: well on die VTH function is enabled.

PCH (3/8):DMI/FDI/PM

Kendo-3 WS

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.
L. DDC_DATA has a weak (20K) internal pull down. When this pin is high at PLTRST# deassertion, LVDS interface is detected.

DDVO_CTRLDATA has internal pull down. When the high is detected at PLTRST# deassertion, Port B is detected. To use Port B, need to add external pull up.

DDPC_CTRLDATA has internal pull down. When the high is detected at PLTRST# deassertion, Port C is detected. To use Port C, need to add external pull up.

DDPD_CTRLDATA has internal pull down. When the high is detected at PLTRST# deassertion, Port D is detected. To use Port D, need to add external pull up.
Because PCI IF is not used, ADx.C/BEx and GNTx are left as NC.

Notes:
- GNTIF has a weak[20K] internal pull up.
- To use SPI if flash BIOS, GNT0/GPIO3 should not be pulled down. If used, GNT0/GPIO3 has a weak[20K] internal pull up.
- This pin should not have external pull down.
- GNT0/GPIO3 has a weak[20K] internal pull up.
- If external pull down is applied, PCI will be "inhibit key" mode.
- USBP0N: To System USB Port (UMA/DSD module)
- USBP1: To System onboard USB port(SATA combo)
- USBP2: To WMX/WLAN Mini Card Slot
- USBP3: To WWAN Mini Card Slot
- USBP4: To SmartCard
- USBP5: To Express Card Slot
- USBP6: Reserved
- USBP7: To Touch Panel
- USBP8: To Color Sensor
- USBP9: To System Subcard USB port
- USBP10: To FPR
- USBP11: To Bluetooth
- USBP12: To Docking
- USBP13: To Camera

Table:

<table>
<thead>
<tr>
<th>Optimus_enable</th>
<th>LVDS/VGA</th>
<th>High</th>
<th>IGPU</th>
<th>Low</th>
<th>DGPU</th>
</tr>
</thead>
</table>

CLKOUT_PCI[4:0] has a internal pull down.

USBP[0:9] has internal pull down. When the pin is high, VCCIO termination function is enabled.

Pin Options:
- GND
- VCC
- Input
- Pull Up
- Pull Down

For RF

- SC12P50V2JN-3GP
- SC100P50V2JN-3GP
- 33R2J-2-GP
- 22R2J-2-GP
- 10KR2J-3-GP
- Do Not Stuff

For USB

- USBP0 to USBP9
- USB0: To System USB Port
- USB1: To System onboard USB port
- USB2: To WMX/WLAN Mini Card Slot
- USB3: To WWAN Mini Card Slot
- USB4: To SmartCard
- USB5: To Express Card Slot
- USB6: Reserved
- USB7: To Touch Panel
- USB8: To Color Sensor
- USB9: To System Subcard USB port
- USB10: To FPR
- USB11: To Bluetooth
- USB12: To Docking
- USB13: To Camera

For PME:

- PME# has internal pullup(20K).
- PME# is high mean SBIOS selection.
When On die PLL function is required, external pull up will not be needed.
LED COLOR should be reversed on the LED board.
Switch Blue

Switch Red

Place near docking connector

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Vendo P/N</th>
<th>WISTRON P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ONSEMI NLASB3157DFT2G</td>
<td>54Y9028CA</td>
</tr>
<tr>
<td>2</td>
<td>Toshiba TC7S3157CFU</td>
<td>73.03157.007</td>
</tr>
<tr>
<td>3</td>
<td>TI 74LVC1G3157DCKRE4</td>
<td>54Y9028BA</td>
</tr>
</tbody>
</table>
Two pins ESD protection diodes are used for R, G, B, VS, HS, DDC_CLK and DDC_DATA lines. Because if three pins ESD protection diodes are used for them, ESD current will rush to VCCCRT and it breaks a VS/HS buffer.

To avoid leak current from a monitor.
NV GPU requires 100K pull-down on AUX signals.

To prevent Leakage current from DP monitor.
Signals can be arranged if there is wiring issue.

Add LVDS MUX on p.36 instead of Dock DP MUX.

NZ-3 uses two of CBT3257ABQ due to space limitation.
NV GPU requires 100K pull-down on AUX signals near GPU.

NV GPU requires 100K pull-down on AUX signals near GPU.
T:EN default state this pin is internally pulled high.
Pericom:EN default state this pin is internally pulled high.

TABLE

<table>
<thead>
<tr>
<th>EN</th>
<th>D0</th>
<th>D1</th>
<th>CH - 0</th>
<th>CH - 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>STANDBY</td>
<td>STANDBY</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>BOOST</td>
<td>STANDARD</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>STANDARD</td>
<td>BOOST</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>BOOST</td>
<td>BOOST</td>
</tr>
</tbody>
</table>

U41
Part Number  R278  R395  R481
1  T1  SN75LVCP412ARTJR-GP  71.75412.A03  NO ASM  10K  0
2  Pericom  P1EQX4951STZDEX-GT  71.34951.A03
3  T1  SN75LVCP412CD  71.75412.B03  4.7K  NO ASM
2  Pericom  P1EQX6741STBZDE  71.36741.003
1CH USB Power Switch w/o Output Discharge Function

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Vendo P/N</th>
<th>WISTRON P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>TI</td>
<td>TPS2065DGN-GP</td>
</tr>
</tbody>
</table>
There is an amplifier on docking station. This resistor divider is for adjusting amplitude to system microphone.

Place R675 and R819 near Docking Conn.

Place under CX20672

Place NEAR SPEAKER CONN

Taping

Place NEAR CODEC

(At least 20mil)

MIC IN
ENABLE

Macro WSN/ENABLE/UNUSED

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Vendor Part Number</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>OnSem</td>
<td>68V5F47A</td>
<td>48V5F47A</td>
</tr>
<tr>
<td>ROHM</td>
<td>105S008</td>
<td>48V5F47A</td>
</tr>
<tr>
<td>NXP</td>
<td>PESD40V015</td>
<td>48V5F47A</td>
</tr>
</tbody>
</table>
Do we need 1.5A fuse on this power rail?
NOTE: VCC1R05LAN WILL WORK AT 0.95V TO 1.15V
When PCIe IF device does not use, these signals will be removed.

On WWAN Always on regular mode. This component has to be assembled, instead of above D+D-jumper.

For RF, place near WLAN slot

For RF, place near WWAN slot

---

<table>
<thead>
<tr>
<th>WWAN</th>
<th>YES</th>
<th>NO</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN12</td>
<td>ASM</td>
<td>No_ASM</td>
</tr>
<tr>
<td>J7</td>
<td>ASM</td>
<td>No_ASM</td>
</tr>
<tr>
<td>C567</td>
<td>ASM</td>
<td>No_ASM</td>
</tr>
<tr>
<td>C565</td>
<td>ASM</td>
<td>No_ASM</td>
</tr>
<tr>
<td>C568</td>
<td>ASM</td>
<td>No_ASM</td>
</tr>
<tr>
<td>C2018</td>
<td>ASM</td>
<td>No_ASM</td>
</tr>
</tbody>
</table>
EXC POWER IC has internal PU for
PIN#9(-CPUSB), PIN#10(-CPPE)

PU is placed on PCH page.
The circuit is required for Kendo-3 since it is possible to connect AC adapter to the system even if docked.
Necessity of R198 depends on location of H8

Check H8 source to perform maxpower management
Power rail for R510 can be either VCCSB or VCCSB.

PU on LID_SWITCH_EC is required. PE in WKS does not have LID sensor but needs to use LCD panel.

System Detection using external strap on Kendo-3

<table>
<thead>
<tr>
<th>#13 PGPIO3 of Thinker-1(U59)</th>
<th>UMA</th>
<th>SWG</th>
<th>WS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

#35 VIDEO_ID of HB(U35B)

<table>
<thead>
<tr>
<th>UMA</th>
<th>SWG</th>
<th>WS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

Table

<table>
<thead>
<tr>
<th>GFX</th>
<th>EXT.</th>
<th>INT.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASM</td>
<td>NO_ASM</td>
<td>A2D</td>
</tr>
<tr>
<td>NO_ASM</td>
<td>A2D</td>
<td></td>
</tr>
</tbody>
</table>

plz modify this logic table

LOGIC

plz modify this logic table

LOGIC

TEST PAD X2

BOTTOM SIDE

DO NOT MOVE AFTER FIX

H8 12C BUS2

Do Not Move

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Width = 6 mil & Spacing = 10 mil for three Output traces

Layout Comment:

1. Place C586, C588, Q17, R415, R417, C584, C585, R420 close to U34.
2. Avoid routing under DCDC switching area.
Need to check control way of DCDC circuits
Sensor Device | Placed on
--- | ---
S0 (Body) | PCH/BASE COVER (Bottom)
S1 | GFX_D (Top)
S2 | GBE (Bottom)
S3 | WWAN (Top)
S4 | DIMM (TOP) (Top)
S5 | DIMM (BOT) (Bottom)
S6 | WLAN (Top)
S7 | EXPRESS SLOT (Bottom)

Resistor Value | SMBUS Address
--- | ---
GND | 1001 100, 4Ch
270 | 1001 101, 4Dh
560 | 1001 110, 4Eh
1K | 1001 111, 4Fh
1.5K | 1001 001, 49h
2.7K | 1001 010, 4Ah
5.6K | 1001 011, 4Bh
>=18K | 0011 000, 18h

Sensor Location will be decided based on the placement.

Layout Comment:
1. Thermal sensor trace lines should not be overlapped with other high frequency trace lines in other layers.
2. Also, it should not be overlapped with large amplitude trace lines either.
VOUT = 0.249 (V_{BAT} - 5)
Table

<table>
<thead>
<tr>
<th>CONSTANT CONNECT</th>
<th>YES</th>
<th>NO</th>
</tr>
</thead>
<tbody>
<tr>
<td>D72</td>
<td>ASM</td>
<td>NO_ASM</td>
</tr>
</tbody>
</table>

Placed close to VT1316M
Place these MLCC Caps symmetrically on Top and bottom.

RF team request

Do Not Stuff

RF team request

Do Not Stuff
These circuits are optimized for Quad Core CPU. When Dual Core will be used, need to change the phase count and QTY of output capacitors.
BLANK
This circuit is used for Integrated GFX power.
If Integrated GFX does not use, No need to assemble.
<table>
<thead>
<tr>
<th>VOUT</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.10V</td>
<td>R_VDES = 40.2K</td>
</tr>
<tr>
<td>1.05V</td>
<td>R_VDES = 38.3K</td>
</tr>
</tbody>
</table>

VOUT = 1.212 \times \frac{R_{VDES}}{44.2K}

Place these filter near U128

VCC_SENSE Trace should rout to VSS_VSENSE in Parallel.

Change to VT356

(74.00356.A3Z)

(Keep VT358 pad)
Place these filter near U127

VSENSE-(VDES) Trace should rout to VSENSE+ in Parallel.
Vout = 2V * (R2 / (R1 + R2))
Place these filter near U151

VCCSA power output is controlled by VCCSA_SEL.
This signal is Low : VCCSA output is 0.9V.
This signal is high (1.05V) : VCCSA output is 0.8V.

VCCSA = 0.9V/0.8V

VCCSA_SENSE Trace should rout to VSSSA_SENSE in Parallel.
Place caps close to pin 126 as possible.

SPD Address: 52h

This connector should be placed on near side from CPU.
This connector should be placed on near side from CPU.
SODIMM should be installed on CH0 Primary at first.

Pin 1 on SODIM connector (VREF_DQ) only connects to DDR Voltage divider.

Clarksfield H17/J17 is left.

SODIMM HIC Address:
- CH-A Primary: 50h
- CH-B Primary: 51h
- CH-A Secondary: 52h
- CH-B Secondary: 53h
DG requires 4x0.1μF and 8x1.0μF per VRAM chip.
Long power trace EMI decoupling caps

VCC1R5A

C182
SCD1U16V2KX-3GP

C181
SCD1U16V2KX-3GP

VCC1R5B

C180
SCD1U16V2KX-3GP

C168
SCD1U16V2KX-3GP

VCC1R05LAN

C248
SCD1U16V2KX-3GP

C249
SCD1U16V2KX-3GP

VCC5M

C273
SCD1U16V2KX-3GP

C275
SCD1U16V2KX-3GP

VCCGFXCORE_D

C291
SCD1U16V2KX-3GP

VCC3M

C250
SCD1U16V2KX-3GP

C252
SCD1U16V2KX-3GP

VCCCPUCORE

C272
SCD1U16V2KX-3GP

C278
SCD1U16V2KX-3GP

C282
SCD1U16V2KX-3GP

C279
SCD1U16V2KX-3GP