### RESISTOR

<table>
<thead>
<tr>
<th>Symbol name</th>
<th>Value</th>
<th>Tolerance</th>
<th>Rating</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>10KR3</td>
<td>10K Ohm</td>
<td>0.1%</td>
<td>1/16W, 75V</td>
<td>0603</td>
</tr>
<tr>
<td>332R5</td>
<td>33.3 Ohm</td>
<td>0.1%</td>
<td>1/10W, 100V</td>
<td>0605</td>
</tr>
<tr>
<td>1KR3</td>
<td>1K Ohm</td>
<td>F: 1%</td>
<td>1/16W, 75V</td>
<td>0603</td>
</tr>
</tbody>
</table>

- The naming rule is value + R + size + tolerance
- For the value, it can be read by the number before R (R means resistor)
- For the tolerance, it can be read from the last letter.
- For the rating, we don’t show on the symbol name.
- For the size, R2=>0402, R3=>0603, R5=>0805....

### CAPACITOR

<table>
<thead>
<tr>
<th>Symbol name</th>
<th>Value</th>
<th>Tolerance</th>
<th>Rating</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCD1U10V2M1X</td>
<td>0.1uF</td>
<td>M/X5R</td>
<td>10V</td>
<td>0402</td>
</tr>
<tr>
<td>SCD1U10V2M1X</td>
<td>10uF</td>
<td>M/X5R</td>
<td>6.3V</td>
<td>0805</td>
</tr>
<tr>
<td>SCD1U10V2M1X</td>
<td>2.2uF</td>
<td>Z/Y5V</td>
<td>16V</td>
<td>0605</td>
</tr>
</tbody>
</table>

- The naming rule is capacitor type + value + rating + size + tolerance + material
- SCD1U10V2M1X-1
  - SCD=> SMT Ceremic, TC=> POS cap or SP cap
  - D1U => 0.1uF
  - 10V => the voltage rating is 10V
  - 2=>0402, 3=>0603, 5=>0805
  - M=tolerance M, K, Z
  - X=>X7R/X5R, Y=>Y5V
  - -1 => symbol version, nonsense to EE characteristic

### PLANAR ID[3:0]

<table>
<thead>
<tr>
<th>PLANAR ID (3:0)</th>
<th>Planar ID Version</th>
<th>Planar PCB Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCH_ID (3:0)</td>
<td>39 38 37 36</td>
<td>48</td>
</tr>
</tbody>
</table>

- The naming rule is value + R + size + tolerance
- For the value, it can be read by the number before R (R means resistor)
- For the tolerance, it can be read from the last letter.
- For the rating, we don’t show on the symbol name.
- For the size, R2=>0402, R3=>0603, R5=>0805....

### PCI TABLE

<table>
<thead>
<tr>
<th>DEVICE (Default)</th>
<th>PCIe (Default)</th>
<th>REG1/3GS</th>
<th>REG2/4GS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINI Slot</td>
<td>AD16</td>
<td>F, G</td>
<td>REQ#3/ GNT#3</td>
</tr>
<tr>
<td>CARDBUS 5/8</td>
<td>AD16</td>
<td>SERIRQ</td>
<td>REQ#3/ GNT#3</td>
</tr>
<tr>
<td>USB UHCI</td>
<td>AD29</td>
<td>A, C, D</td>
<td>-</td>
</tr>
<tr>
<td>USB 2.0 EHCI</td>
<td>AD29</td>
<td>H</td>
<td>-</td>
</tr>
<tr>
<td>SMII-PCI</td>
<td>AD30</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>LPC Bridge</td>
<td>AD31</td>
<td>C</td>
<td>B</td>
</tr>
<tr>
<td>PCI Express</td>
<td>AD29</td>
<td>A, B, C, D</td>
<td>-</td>
</tr>
</tbody>
</table>
Trace Width and length should be designed based on Intel Platform design guide. Please see Doc No 29635 page 73.

These Pins can be floated.
Need to refer Intel Design Guide to place CPU and route wire.

SKTOCC# pin is tied down by CPU, when CPU is inserted at socket.

Catastrophic error output is not used.

This test point is used at PCBA process.

This test point is used at PCBA process.

Need to find Schmitt with Open drain output

U98 Place near CPU

This change is to S3 Wake up issue based on Intel White paper
Ivy Bridge QC/XE can provide VREF power for DDR3 interface.
Should be add pull down 1K based on configuration specification.

When PEG Lane reversible function is used, CFG2 should have pull down.

When PCIe Port Bidirectional function is used, CFG5 & 6 should have pull down.

Low/High : x8, x4 and x8
Low/High : Reserved
High/High : x16

Test point on CFG1, CFG3-CGF7, CFG16 are for Intel CPU debugging.
### SIGNAL REF DES ENABLE DISABLE

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>REF DES</th>
<th>ENABLE</th>
<th>DISABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDO</td>
<td>R475</td>
<td>ASM</td>
<td>NOASM</td>
</tr>
<tr>
<td>TRST#</td>
<td>R471</td>
<td>ASM</td>
<td>ASM</td>
</tr>
<tr>
<td>DBRST#</td>
<td>R491</td>
<td>ASM</td>
<td>ASM</td>
</tr>
<tr>
<td>RESET#</td>
<td>R588</td>
<td>ASM</td>
<td>ASM</td>
</tr>
<tr>
<td>CFG0</td>
<td>R477</td>
<td>ASM</td>
<td>NOASM</td>
</tr>
<tr>
<td>PWRGD</td>
<td>R594</td>
<td>ASM</td>
<td>NOASM</td>
</tr>
<tr>
<td>BPWRG</td>
<td>R954</td>
<td>ASM</td>
<td>NOASM</td>
</tr>
<tr>
<td>CN18</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### DEBUG Interface for PCH.

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>REF DES</th>
<th>ENABLE</th>
<th>DISABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDO</td>
<td>R509</td>
<td>220</td>
<td>NOASM</td>
</tr>
<tr>
<td>TMS</td>
<td>R530</td>
<td>220</td>
<td>NOASM</td>
</tr>
<tr>
<td>TDI</td>
<td>R515</td>
<td>220</td>
<td>NOASM</td>
</tr>
<tr>
<td>TCK</td>
<td>R541</td>
<td>51</td>
<td>51</td>
</tr>
<tr>
<td>MPWRG</td>
<td>R511</td>
<td>ASM</td>
<td>ASM</td>
</tr>
<tr>
<td>CN19</td>
<td></td>
<td>ASM</td>
<td>NOASM</td>
</tr>
</tbody>
</table>

**In production, All of parts should be not mounted except of pulldown 51 ohm on TRST# and Pullup DBR#**.

**CPU XDP SFF 26pin IF**
- Pin 1 OBSFN_A0 (PREQ#, I/O)
- Pin 2 OBSFN_A1 (PRDY#, I/O)
- Pin 3 GND
- Pin 4 OBSDATA_A0 (Open, I/O)
- Pin 5 OBSDATA_A1 (Open, I/O)
- Pin 6 GND
- Pin 7 OBSDATA_A2 (Open, I/O)
- Pin 8 OBSDATA_A3 (Open, I/O)
- Pin 9 GND
- Pin 10 HOOK0 (PWRGD, In)
- Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
- Pin 12 HOOK2 (CFG0, Out)
- Pin 13 HOOK3 (BP_PWRGD_RST#, Out)
- Pin 14 HOOK4 (BCLK, In)
- Pin 15 HOOK5 (BCLK, In)
- Pin 16 VCCOBS_A (VCCP Voltage of CPU, In)
- Pin 17 HOOK6 (RSMRST#, Out)
- Pin 18 HOOK7 (DBR#, Out)
- Pin 19 GND
- Pin 20 TDO, In
- Pin 21 TRST# (Out)
- Pin 22 TDI, Out
- Pin 23 TMS, Out
- Pin 24 TCK1 (Open)
- Pin 25 GND
- Pin 26 TCK2 (Out)

**In production, All of parts should be not mounted except of pulldown 51 ohm on TCK.**

**Wistron Corporation**

1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
SODIMM IC Address:
CH-A Primary [DIMM1]: 56h
CH-B Primary [DIMM3]: 54h
CH-A Secondary [DIMM2]: 52h
CH-B Secondary [DIMM1]: 53h

Please see SODIMM Configuration in Page 102
ODIMM IIC Address:

CH-A Primary (DIMM4): 50h
CH-B Primary (DIMM3): 51h
CH-A Secondary (DIMM2): 52h
CH-B Secondary (DIMM1): 53h

MB_CLK_3B 12,34,64,70,104,105

Please copy close to pin to ease possible setup configuration.

This connector should be placed on far side from CPU.
220ohm@100MHz ESR=0.05ohm

20mA

www.Laptopblue.vn

Need 10mil thickness signal and 10mil GND guard

GP1012 for power control

<table>
<thead>
<tr>
<th>DEV</th>
<th>DIV-A</th>
<th>FVT</th>
<th>FVT-2nd</th>
<th>SIT</th>
<th>SIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>U125</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
</tr>
</tbody>
</table>

I2CA=>CRT, I2CC=>LVDS.

TABLE LEDO NVIDIA

<table>
<thead>
<tr>
<th>LEDO</th>
<th>DIV-A</th>
<th>FVT</th>
<th>FVT-2nd</th>
<th>SIT</th>
<th>SIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV</td>
<td>DIV-A</td>
<td>FVT</td>
<td>FVT-2nd</td>
<td>SIT</td>
<td>SIT</td>
</tr>
<tr>
<td>U125</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
<td>DEV ID:</td>
</tr>
</tbody>
</table>

TABLE VIDEO MEMORY

| HYNIX | SAMSUNG | SAMSUNG |
| 128Mx16 | 128Mx16 | 128Mx16 |
| 0110 | C-DIE 0111 | E-DIE 0100 |

ROM_SIPD

RS597

34.8Kohm

45.3Kohm

24.9Kohm
### TABLE

<table>
<thead>
<tr>
<th>HYMNIX 2GBITS (128MX16) NEW DIE</th>
<th>SAMSUNG 2GBITS (128MX16) NEW DIE</th>
</tr>
</thead>
<tbody>
<tr>
<td>U100 U111</td>
<td>J99 U108</td>
</tr>
<tr>
<td>J107 U110</td>
<td>J105 U109</td>
</tr>
<tr>
<td>MT41J256M16RE-107-D-GP</td>
<td>HSTQG63DFR-11C</td>
</tr>
<tr>
<td>K4WZ61646E-BC11</td>
<td></td>
</tr>
</tbody>
</table>

### FB CMD mapping Mode D-N12c

#### FOR U100/U99

CLOSE TO THE MEMORY

#### FOR U107/U105

CLOSE TO THE MEMORY

---

*Bonus Information*

- **istron Corporation**
  2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

- **Website**: [www.Laptopblue.vn](http://www.Laptopblue.vn)
No need External device.(integrated pull down is enabled.) When On die VR for 1.5V is required, Need to add external pull up.

HDA_RST# has a weak(20K) internal pull down.

SATA1: To ODD Bay

Place close to HDD connector

SATA_LED# has a weak(20K) internal pull up.

SMT0806 pin should have pull up resistor to enable integrated 1.5V VRM.

Length < 0.5"
DDC_DATA has a weak[20K] internal pull down. When this pin is High at PLTRST# deassertion, LVDS interface is detected.

SDVO_CTRLDATA has internal pull down. When the high is detected at PLTRST# deassertion, Port B is detected. To use Port B, need to add external pull up.

DDPD_CTRLDATA has internal pull down. When the high is detected at PLTRST# deassertion, Port D is detected. To use Port D, need to add external pull up.
Because PCI IF is not used, ADx.C/BEx and GNTx are left as NC.

USB 3.0 ports assignment:
Port 0: Left Side Double Deck connector (Upper)
Port 1: Left Side Double Deck Connector (Lower)
Port 2: Docking Connector

**TABLE**

<table>
<thead>
<tr>
<th>OPTIMUS_ENABLE</th>
<th>LVDS/VGA</th>
<th>HIGH</th>
<th>IGP</th>
<th>LOW</th>
<th>DGPU</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**PLTST# distribution List**

FAR ->
- CPU Socket
- XDP [Connector]
- Multi Touch [LED Card IF]
- GBE [Chip]
- WWAN/nSDATA Slot
- WLAN Slot
- NEAR ->
  - MediaCard Reader [Chip]
  - Express Slot Power [Chip]
  - Golden Finger [Card edge]
  - Lenovo Debug port [Connector]
  - Embedded Controller [Chip]
  - Think Engine [chip]
  - TPM [Chip]

**USB**
- USB 0: To System USB Double-Deck Port Upper (USB 3.0 capable)
- USB 1: To System USB Double-Deck Port Lower (USB 3.0 capable)
- USB 2: To Docking (USB 3.0 capable)
- USB 3: To WWAN Mini Card Slot
- USB 4: To System USB Port (AOU Port on USB SubCard)
- USB 5: To Express Card Slot
- USB 6: Color Sensor
- USB 7: To Docking
- USB 8: To SmartCard
- USB 9: To System USB Signal Port
- USB 10: To FFP
- USB 11: To Bluetooth
- USB 12: To WiMAX/WWAN Mini Card Slot
- USB 13: To Camera
When ME TLU confidentiality function is required, External pull up is needed.

GPIO8 has a weak pullup. It is disabled after RSMRST#.
No multiplx with other function and default port setting is InputPort.
No need to apply external pull down/up.

When On the Fly function is required, no need external pull down.
The pull up internal pull up and power on detect is programmed as GPO.
So external pull down will not be needed.

 DATA200/0F10CL, DATA300/0F10T has a weak internal pull down. It is disabled after PFXRST#.

Planar ID table is placed on page 2
Signals can be arranged if there is a wiring issue.

NZ-3 uses two of CBT3257ABQ due to space limitation.
DP CONN
DisplayPort ver.1.2
5.4Gbps supported

POLYSW 6V 1.5A NANOSMDC150F
Typ. 500mA
Max 3A

place near DP connector

Supplier | Vendor P/N | WISTRON P/N |
---------|-------------|-------------|
1        | TOSHIBA T705S057FU | 73.75P57.0AJ |
2        | TI SN74ALVC1G120DSKR | 73.01G12.ANJ |
BLANK
WIRELESS DISABLE SWITCH

On WWAN Always on regular mode. This component have to be assembled, instead of above D+D-jumper.
SD/MMC/MMC+ Card Reader

Close to CARDREADER connector

For EMI Solution.
EXC POWER IC has internal PU for PIN#9(-CPUSB), PIN#10(-CPPE)

PU is placed on PCH page.

www.Laptopblue.vn
Golden Finger for Debug Board

Lenovo Debug Tool IF.

4Mbits SPI FLASH (SPI1):

<table>
<thead>
<tr>
<th>Package</th>
<th>Supplier</th>
<th>Vendor P/N</th>
<th>Lenovo P/N</th>
<th>Wistron P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>SO8</td>
<td>Macronix</td>
<td>MX25L6406EM21-12G</td>
<td>72.2564.0D1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Winbond</td>
<td>W25Q64CVSSIG</td>
<td>72.2564.0B01</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Numonyx</td>
<td>N25Q064A13ESE40F</td>
<td>72.2564.0D01</td>
<td></td>
</tr>
</tbody>
</table>

Trace FIFO debug port

R63  Enable  Disable

32Mbits SPI FLASH (SPI2):

<table>
<thead>
<tr>
<th>Package</th>
<th>Supplier</th>
<th>Vendor P/N</th>
<th>Lenovo P/N</th>
<th>Wistron P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>SO8</td>
<td>Macronix</td>
<td>MX25L3206EM21-12G</td>
<td>72.2532.0C01</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Winbond</td>
<td>W25Q32BVSSIG</td>
<td>72.2532.0A01</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Numonyx</td>
<td>N25Q032A13ESE40F</td>
<td>72.2532.0H01</td>
<td></td>
</tr>
</tbody>
</table>
---DOCK_ATTACHED_BAT_OP--- DISCHARGE

Circuit is required for Kendo-3 since it is possible to connect AC adapter to the system even if docked.

For Lizzie DVI issue

ChiefRiver Platform 104 (Final)

For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)

For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)

For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)

For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)

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For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)

For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)

For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)

For Lizzie DVI issue

ChiefRiver Platform ID# (Pin112)
Power net for KBD backlight is connected to pin 29.
If Direct PWM FAN Module will be pick uped on this project, VCC Pin is needed to FAN Interface connector.

1. VCC
2. PWM
3. FAN_FRQ
4. GND
5. ~ ID
Layout Comment:

(1) Place C586, C588, Q17, R415, R417, C584, C585, R420 close to U34.

(2) Avoid routing under DCDC switching area.

Table:

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Vendo P/N</th>
<th>WISTRON P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ST</td>
<td>LIS34ALTR</td>
<td>74.00034.0BZ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>41R0828AA</td>
</tr>
<tr>
<td>2 Kionix</td>
<td>KXTC8-2850</td>
<td>74.KXTC8.08BZ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>45K0278AA</td>
</tr>
</tbody>
</table>

Width = 6 mil & Spacing = 10 mil for three Output traces.
(1) Thermal sensor trace lines should not be overlapped with other high frequency trace lines in other layers.
(2) Also, it should not be overlapped with large amplitude trace lines either.  

Sensor Location will be decided based on the placement.
When Asset ID function in new EC will be confirmed, These Asset ID and external pull up will be removed. As for Bus Sw, if the requirement is exist, need to keep to prevent current leak.
Present pin has Open drain type output buffer.

Are these signals required for the new charger?
D77:
1st source: ESD523.3TG-ON SEMI
2nd source: uClamp3381H/SEMTECH
VOUT = 0.249 (VBAT - 5)
### Table

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AOAC</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>D73</td>
<td>ASM</td>
<td>NO_ASM</td>
</tr>
<tr>
<td>R902</td>
<td>100K ohm</td>
<td>0 ohm</td>
</tr>
</tbody>
</table>

---

**POWER SEQUENCE**

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

**Title**

Kendo-4 WS

**Date:** Friday, March 09, 2012

**Sheet:** 78 of 106
From CPU
7 VCSENSE

To Controller
VCCCPU_SENSE_VLT

To Controller
VCCGFX_SENSE_I_VLT

From CPU
Cont : 27pcs x 22uF, 10pcs x 10uF
Two-phase Mode
EDP-peak 1.3xEDP-continuous
EDP-continuous 40A

Loadline = zero load-line
Frequency = 300kHz

VDD(6.0)
0.000000 = 1.100V
0.000000 = 1.075V
0.000000 = 1.050V
0.000000 = 1.025V
0.000000 = 1.000V
0.000000 = 0.975V
0.000000 = 0.950V
0.000000 = 0.925V
0.000000 = 0.900V
0.000000 = 0.875V
0.000000 = 0.850V
0.000000 = 0.825V
0.000000 = 0.800V
0.000000 = 0.775V
0.000000 = 0.750V

Boot voltage 0.300V
VDD 0110010

---

District Machine
Wistron Corporation
No. 38, Sec. 1, Heping Road, Xizhi,
Taipei Hsien 221, Taiwan, R.O.C.

Date: Sheet 83

Friday, March 09, 2012
U18: VT357-007/Volterra on VT357-007pad
(74.00356.A32)

VCCSENSE Trace should route to VSS_VSENSE in Parallel.
U28: VT356-007 Volterra on VT357-007 pad (74.00356.A32)

0.5% 1%
VSENSE-(VDES) Trace should rout to VSENSE+ in Parallel.

11A

www.Laptopblue.vn
<table>
<thead>
<tr>
<th>State</th>
<th>S3</th>
<th>S5</th>
<th>VDDR</th>
<th>VTTREF</th>
<th>VTT</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>HL</td>
<td>HL</td>
<td>On</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td>83</td>
<td>Lo</td>
<td>HL</td>
<td>On</td>
<td>On</td>
<td>Off (HL)</td>
</tr>
<tr>
<td>S4/S5</td>
<td>Lo</td>
<td>Lo</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
</tbody>
</table>

For RF debug

CHIP CHOKE 0.56UH ETQP4LR56WFC

DC/DC VCC1R5A/VCC0R75B

Kendo-4 WS

Wistron Corporation
21F, B1, Sec. 1, Nan Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

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Sheet 1 of 1
VCC1R5B discharge circuits at sleep to manage requirement of Intel CPU Power sequence.
18.5kHz
1.008V~1.576V (R223:110kohm): 6.72A~10.5A
where BAT_CURRENT: 150mV/A

TC75S56FE/TOSHIBA (1st source)
BU5265HFV/ROHM (2nd source)
USB_AO_SEL0: High --> Path through mode
USB_AO_SEL0: Low --> Automatic detection mode mode

VCC3LAN
29 - USB_SUBCARD_DTCT

50 - RJ45_LINKUP_SYS
50 - RJ45_ACTIVITY_SYS
28 - USBP4+
28 - USBP4
71 - USB_AO_SEL
71 - USB_ON2
28 - USB_PORT4_OC2

VCCSM

NP2

CN17

SYS_MD1_3+ 50
SYS_MD1_3- 50
SYS_MD1_1+ 50
SYS_MD1_1- 50
SYS_MD1_2+ 50
SYS_MD1_2- 50
SYS_MD1_0+ 50
SYS_MD1_0- 50
SODIMM IIC Address:
CH-A Primary [DIMM4]: 50h
CH-B Primary [DIMM3]: 51h
CH-A Secondary [DIMM2]: 52h
CH-B Secondary [DIMM1]: 53h

SODIMM CH-A

SODIMM CH-B

DQx on Secondary slot are swapped to minimize the trace length and manage routing

Keyboard Side

DDR3-204P-143-GP Channel-A Secondary DDR3-204P-94-GP-U Channel-B Secondary

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Portreplicator

DVI/DP

Dock IF

CRT

LVDS SW

LVDS for LCD

nVidia_GFX N14P

Ivy Bridge

Peg Gen3

Panther Point

FDI

DMI

RGB SW

CRT

Display Port
lace caps close to pin 1 as possible

QC/XE can provide Vref to DIMM

DRAMRST 4,12,13,105

SDRAMST 4,12,13,105

VCC3B

VCC0R75B
SODIMM IC Address:
CH-A Primary (DIMM4): 50h
CH-B Primary (DIMM3): 51h
CH-A Secondary (DIMM2): 52h
CH-B Secondary (DIMM1): 53h

Please see SODIMM Configuration in Page 102